Enso

A Streaming Interface for NIC-Application Communication

Hugo Sadok, Nirav Atre, Zhipeng Zhao, Daniel S. Berger, James C. Hoe, Aurojit Panda, Justine Sherry, Ren Wang

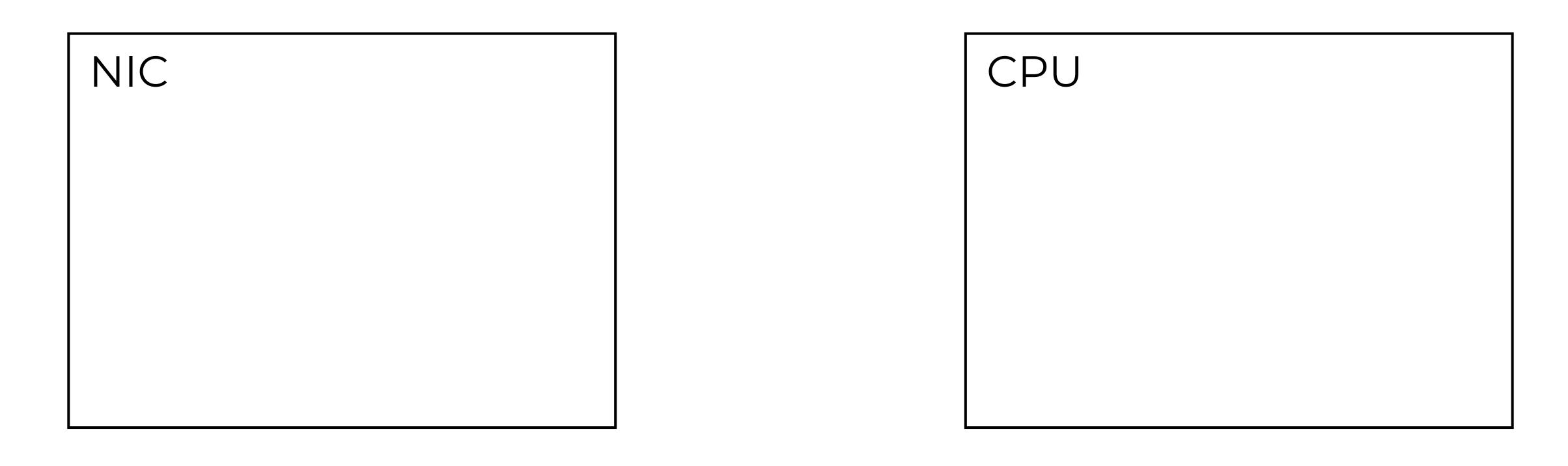


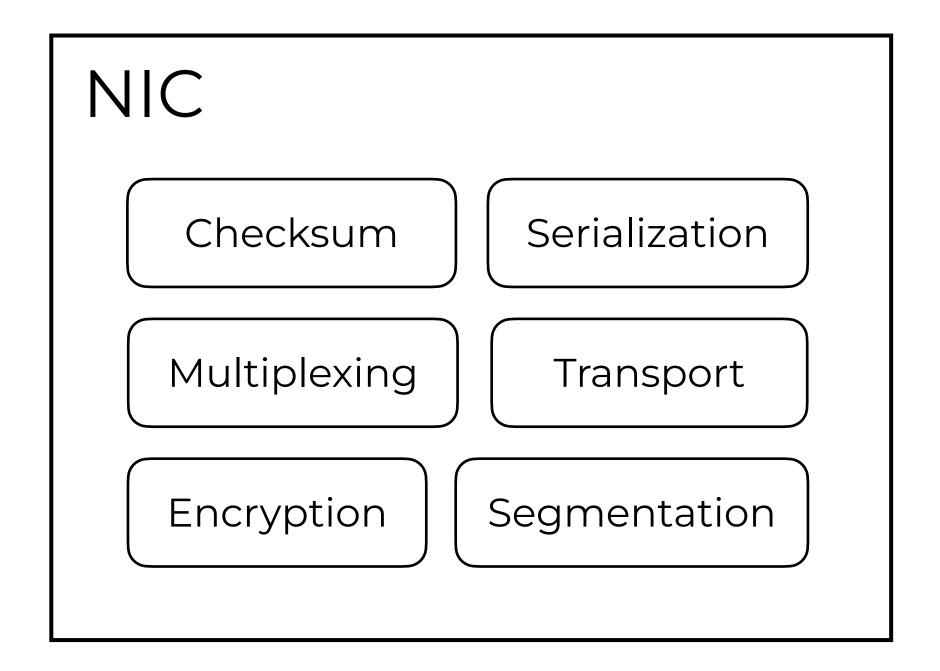




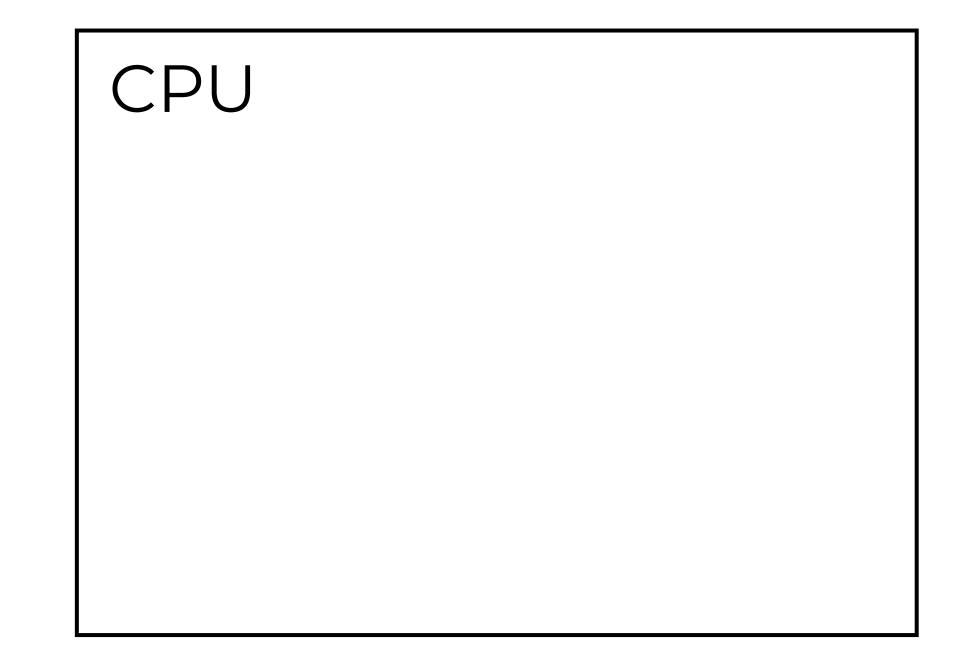


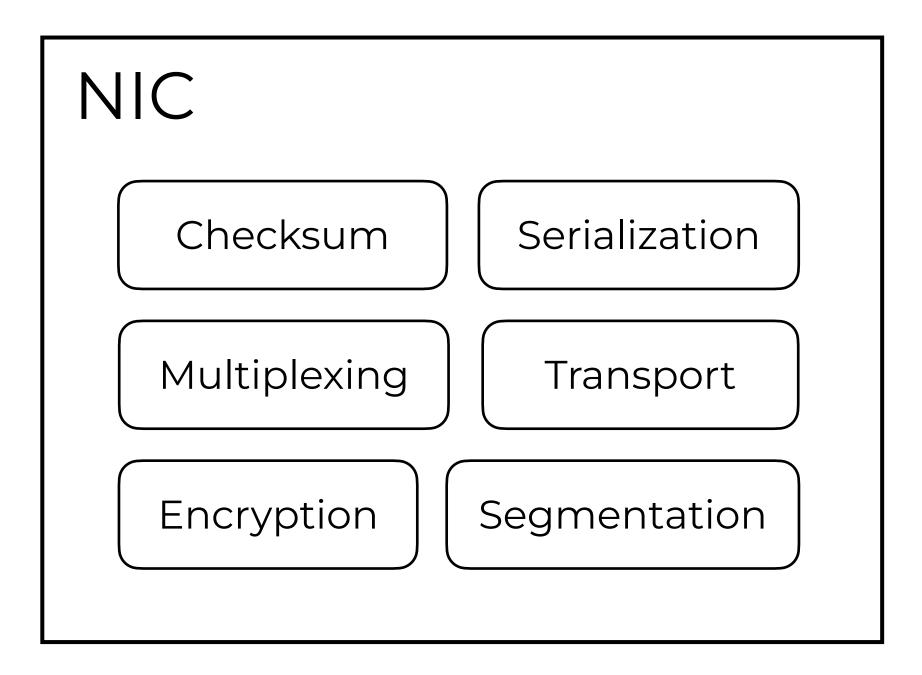






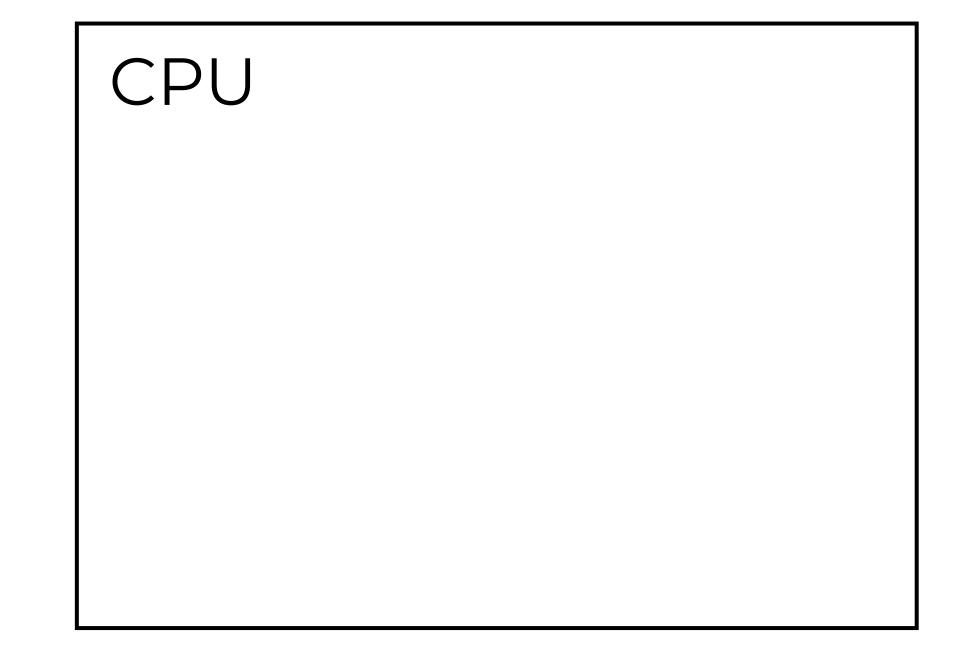
NIC offloads

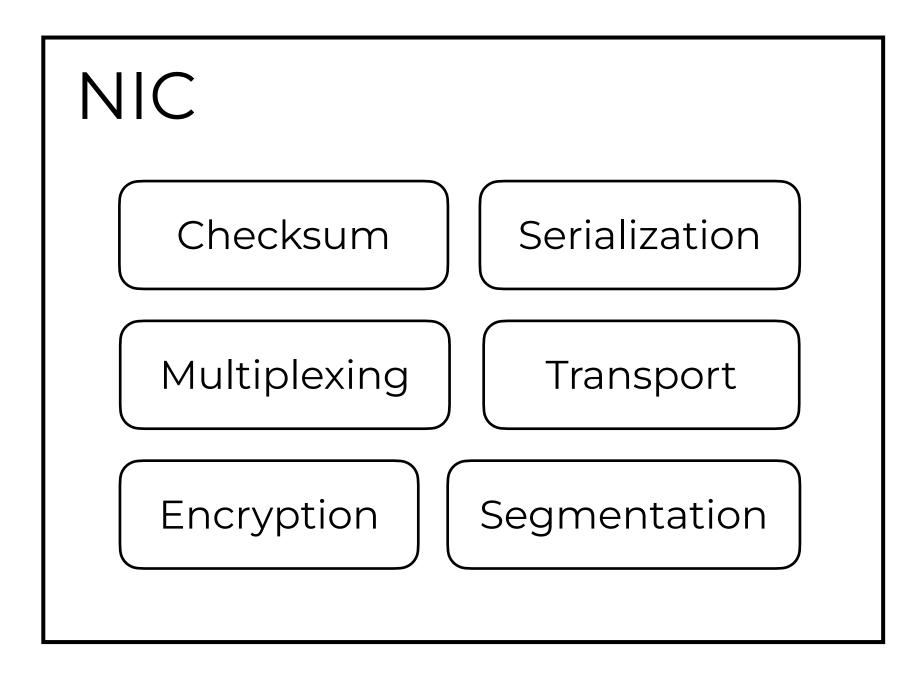




NIC offloads

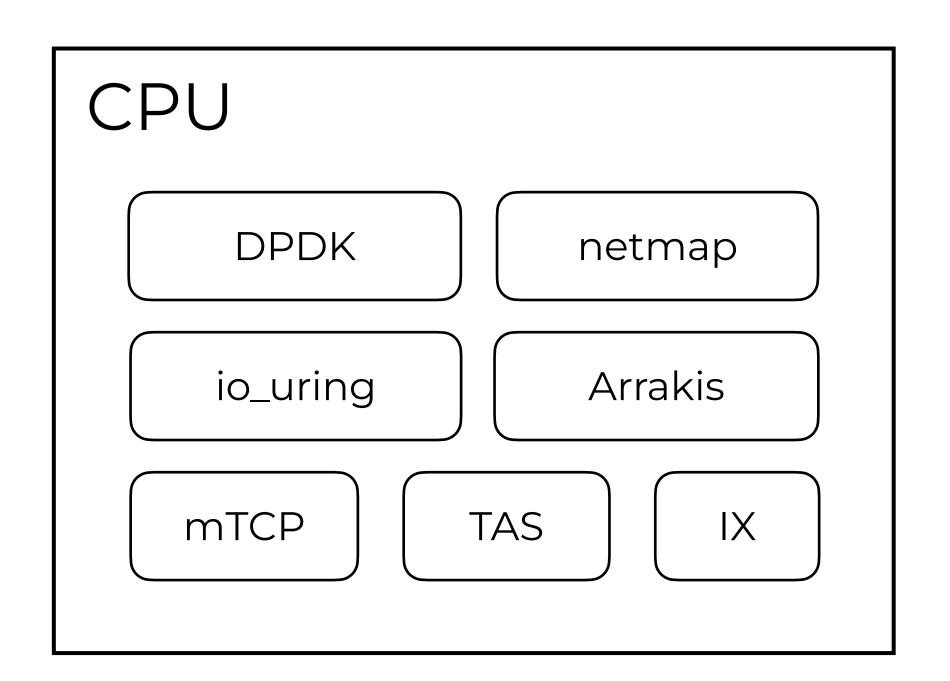
Offloads operate at higher network layers



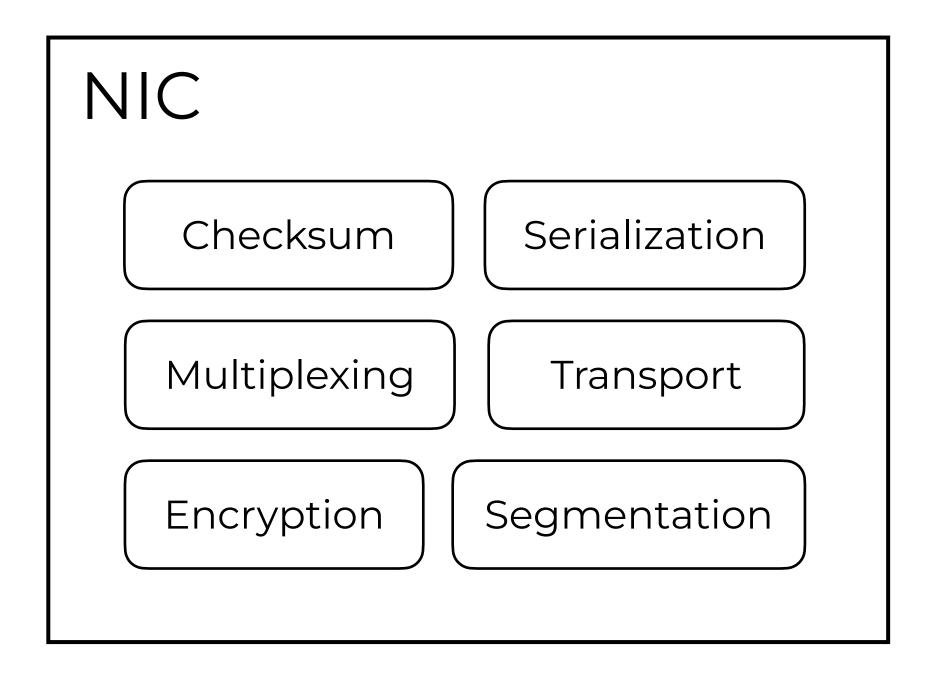


NIC offloads

Offloads operate at higher network layers

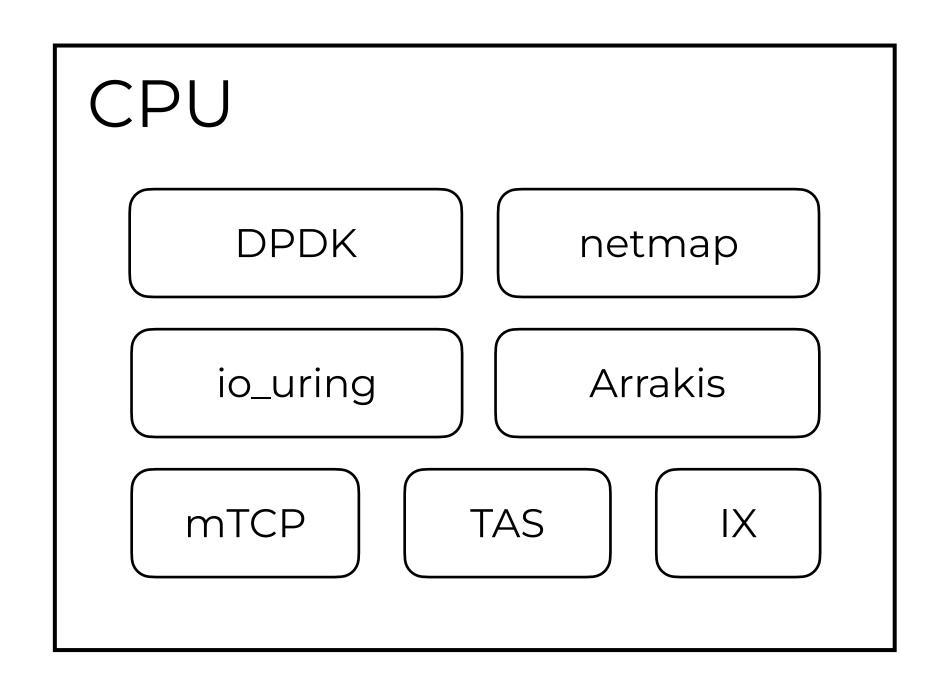


Efficient network stacks



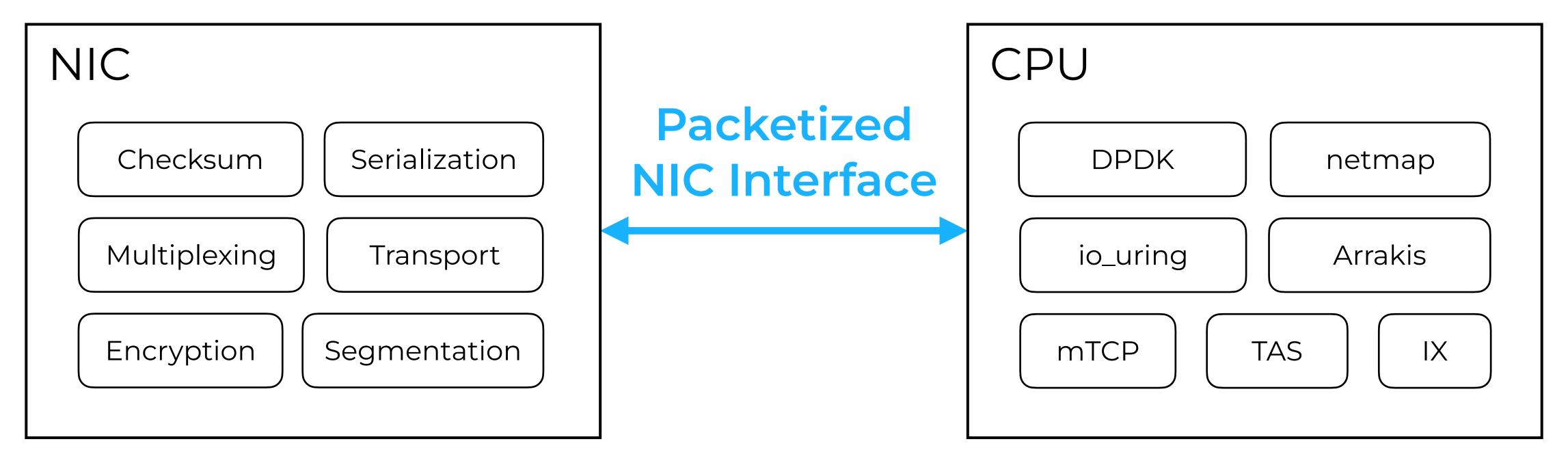
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Offloads operate at higher network layers



Efficient network stacks

Often bypass the kernel and rely on batching



NIC offloads

Offloads operate at higher network layers

Efficient network stacks

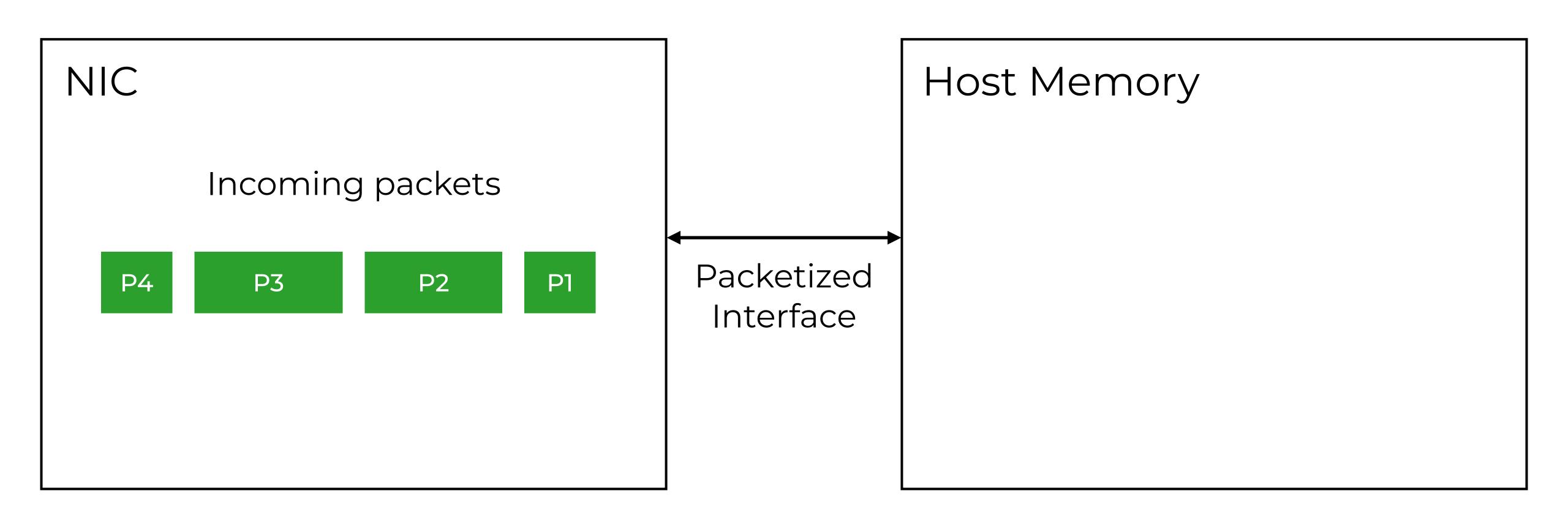
Often bypass the kernel and rely on batching

This Talk:

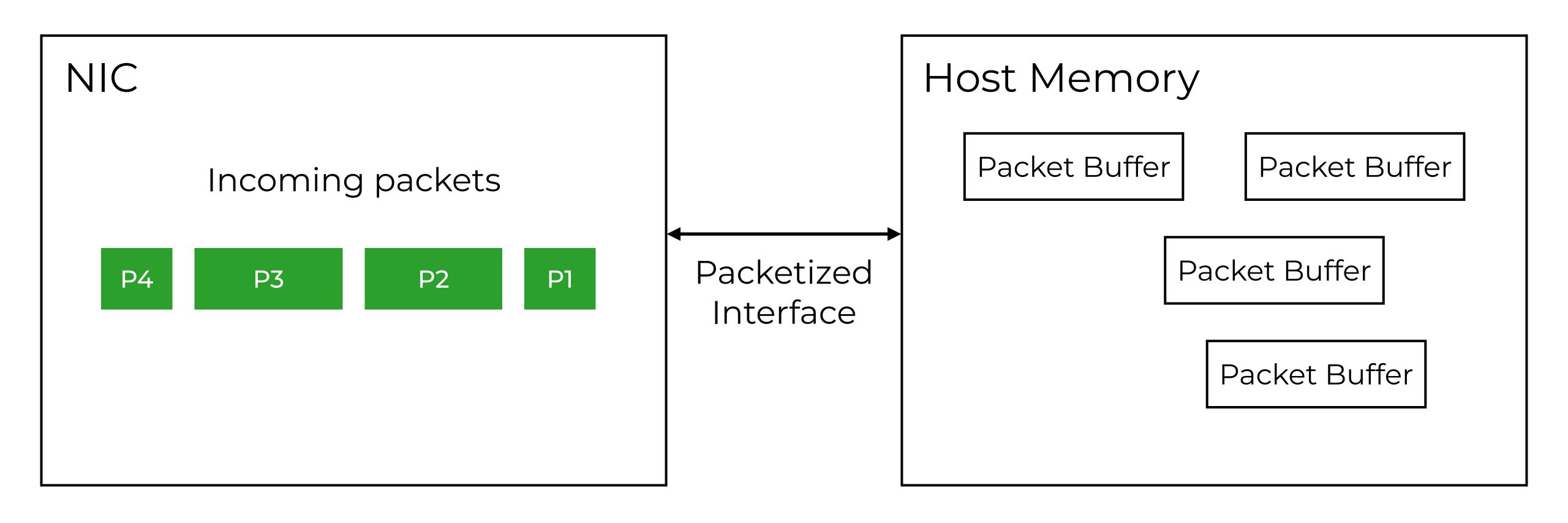
1 Mismatch between how NICs are used and the interface that they provide

Fixing this mismatch can significantly improve performance while paving the way for higher-level offloads

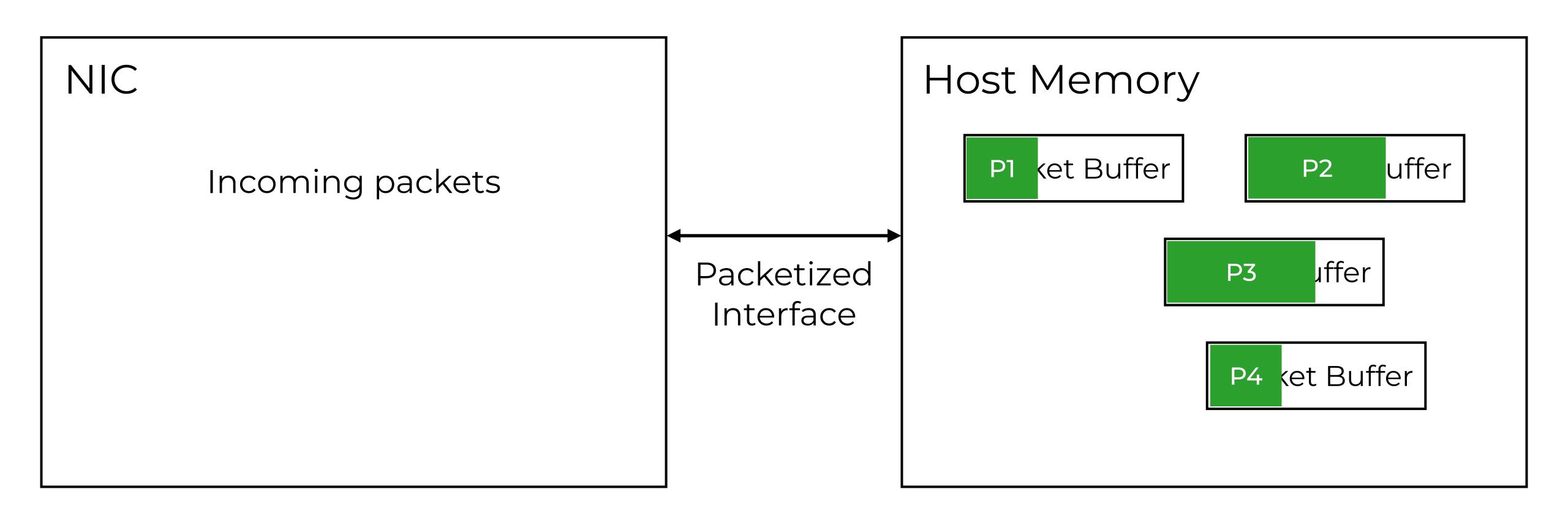
Existing NICs provide a packetized interface

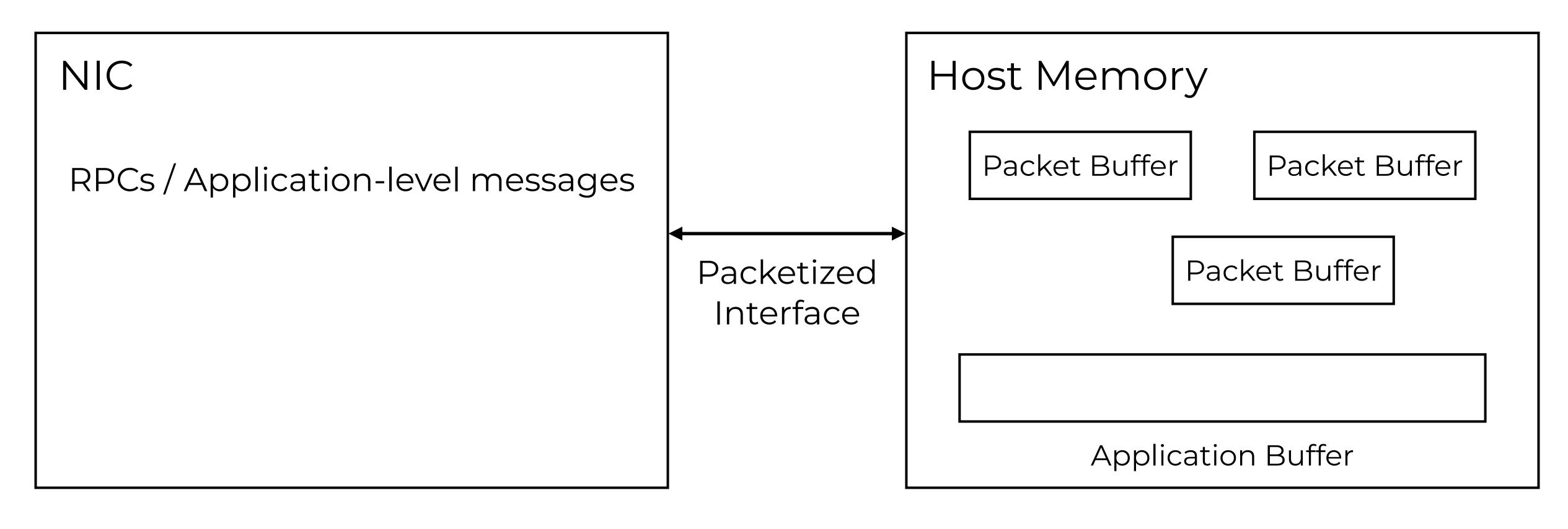


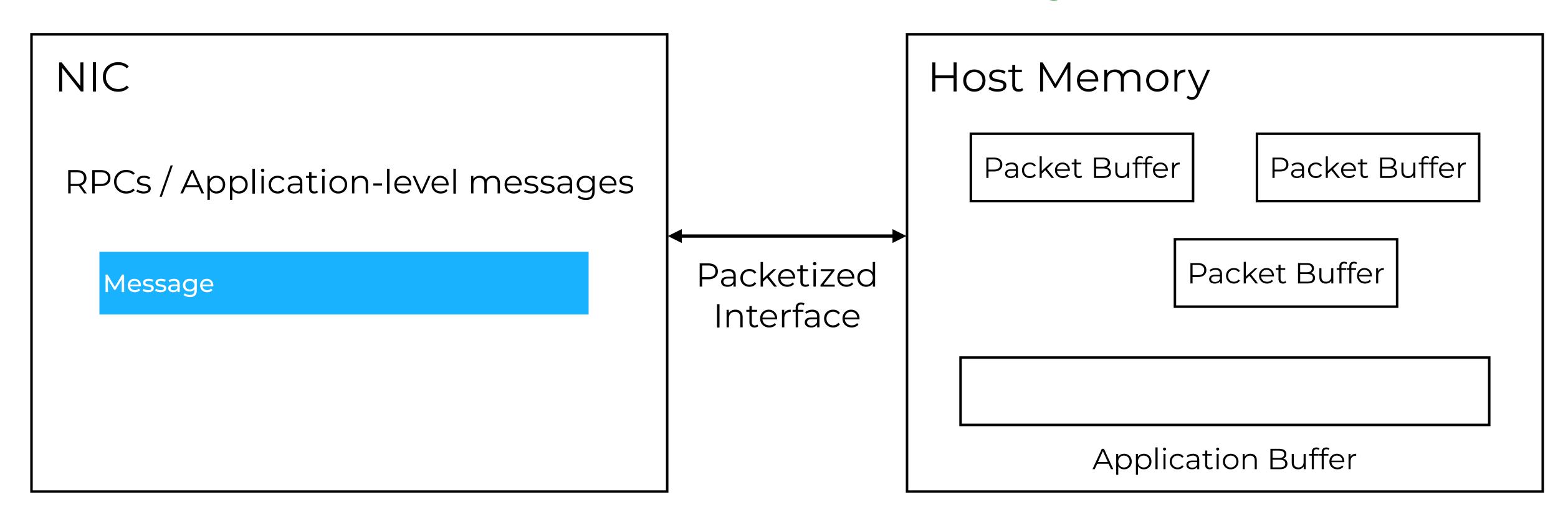
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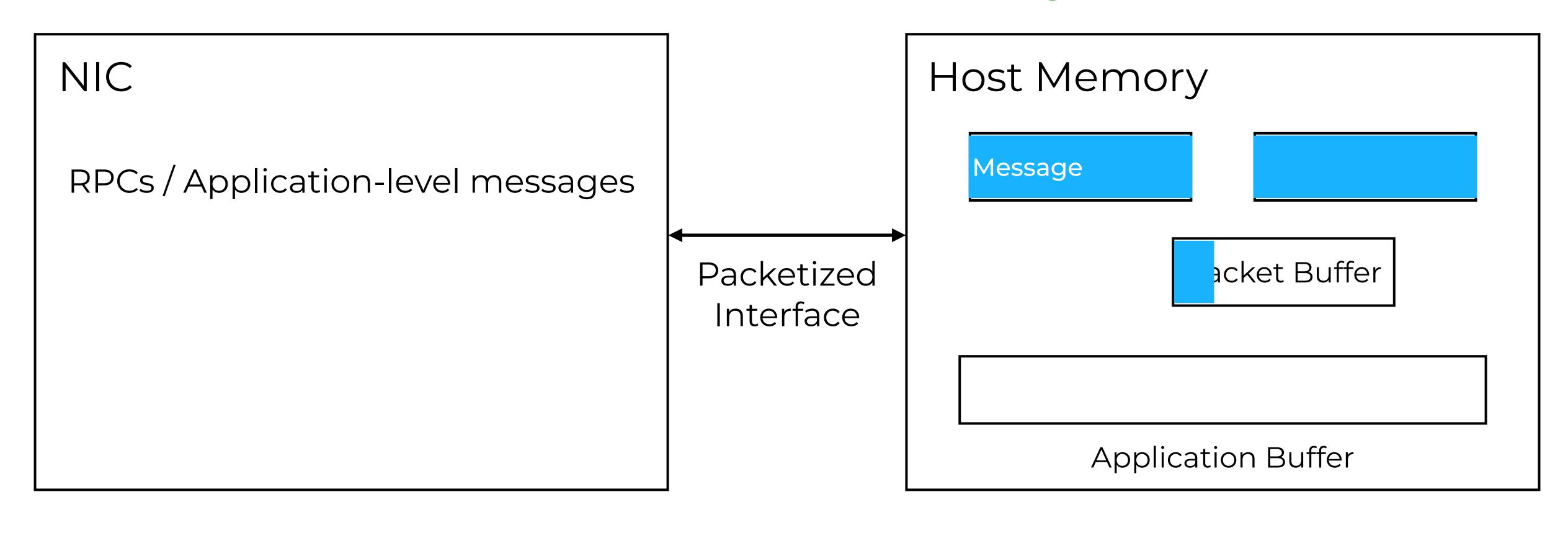


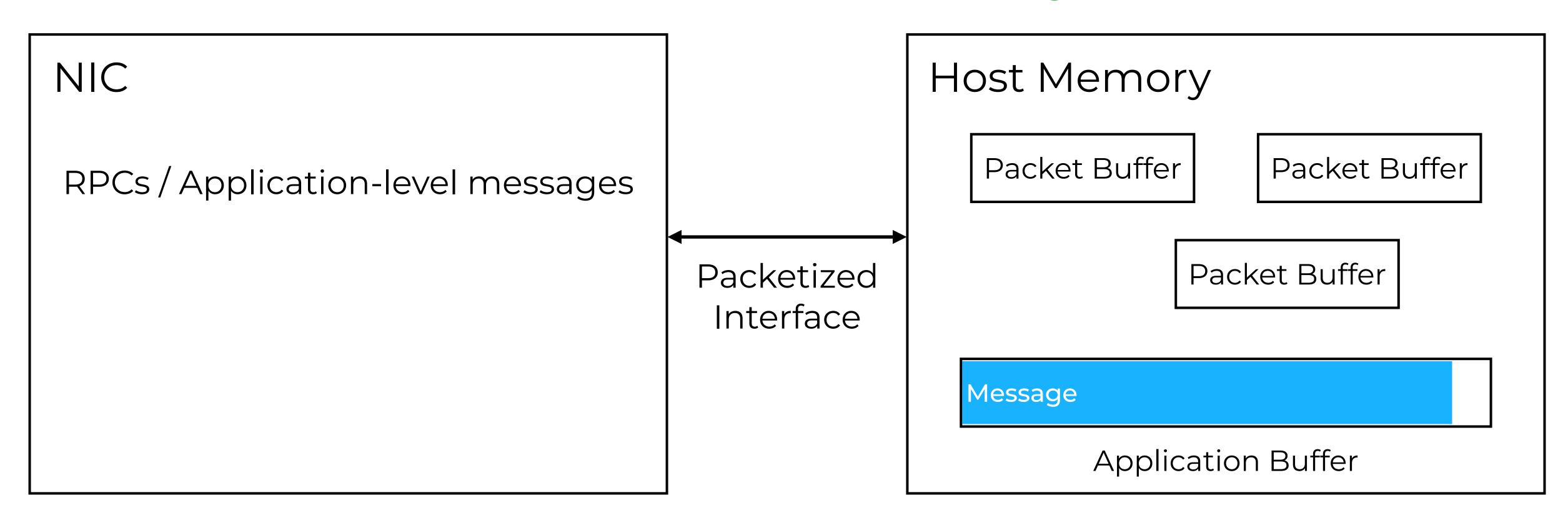
Existing NICs provide a packetized interface

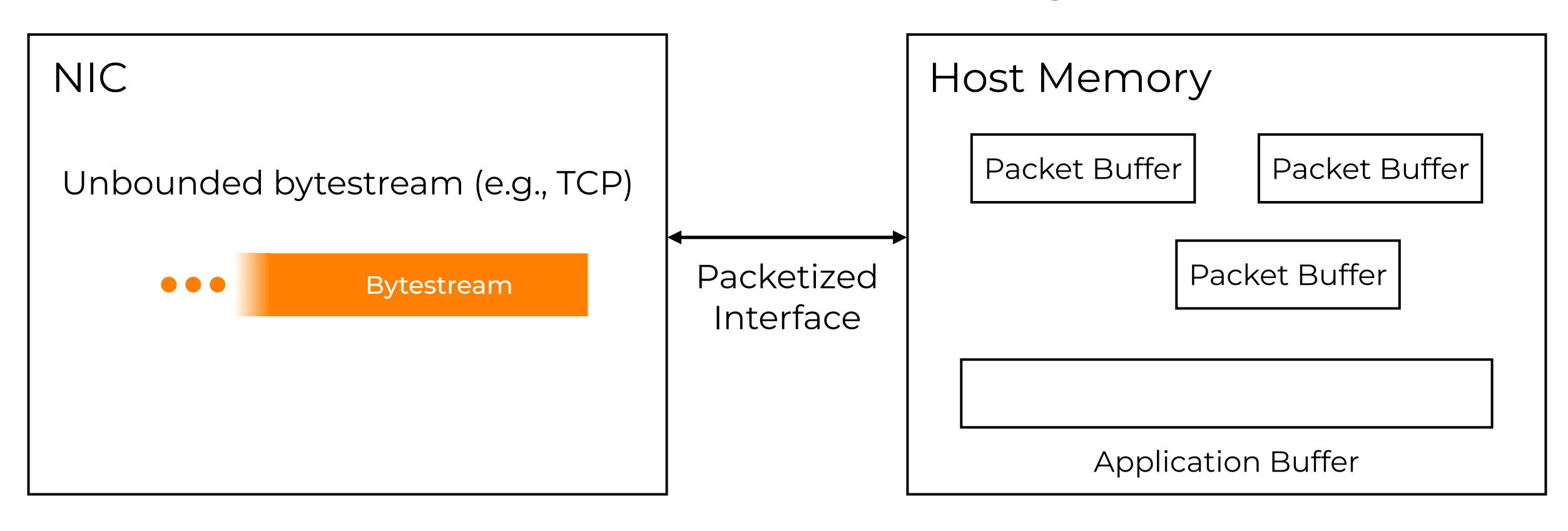


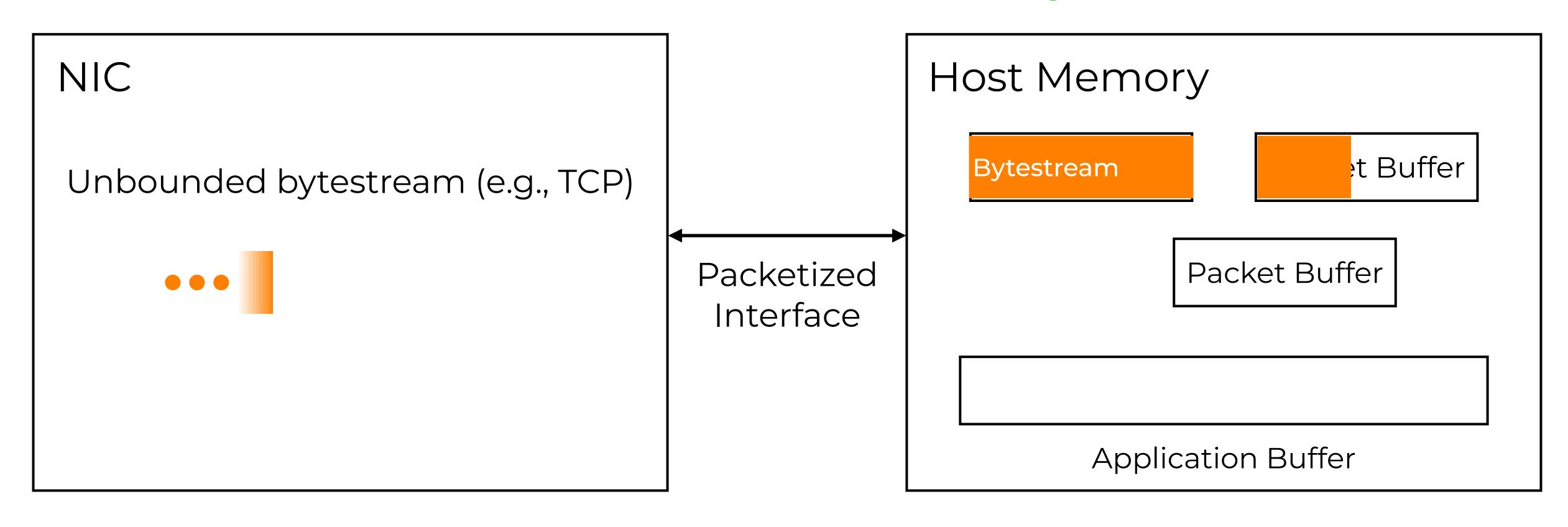


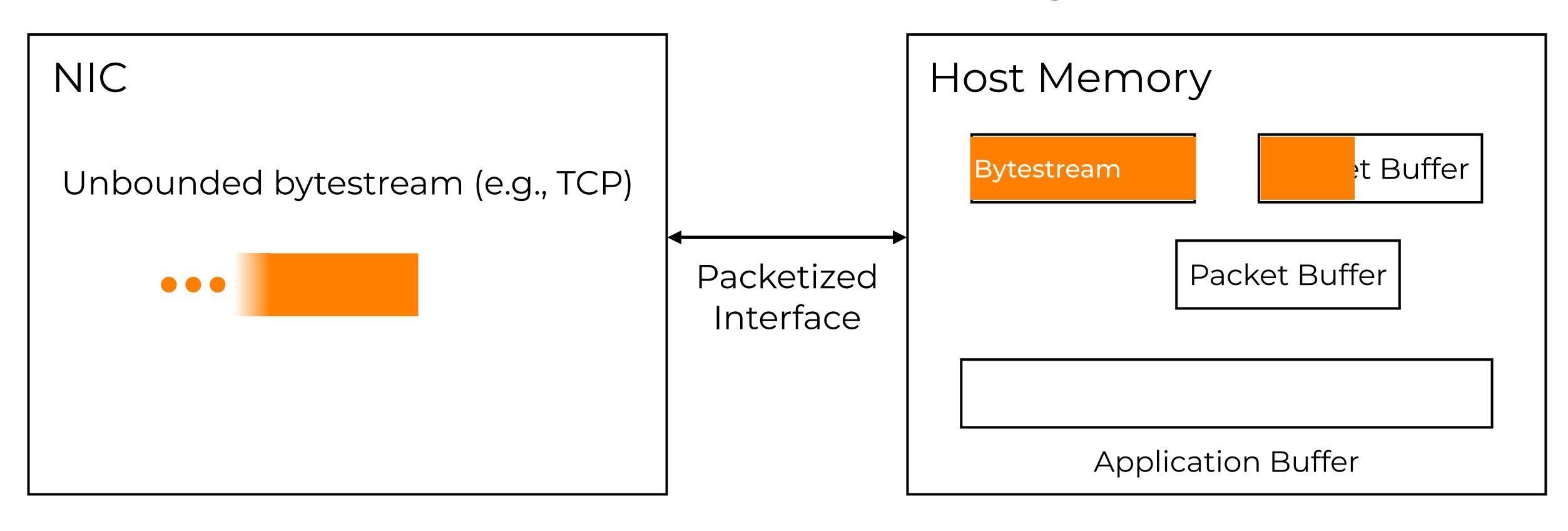


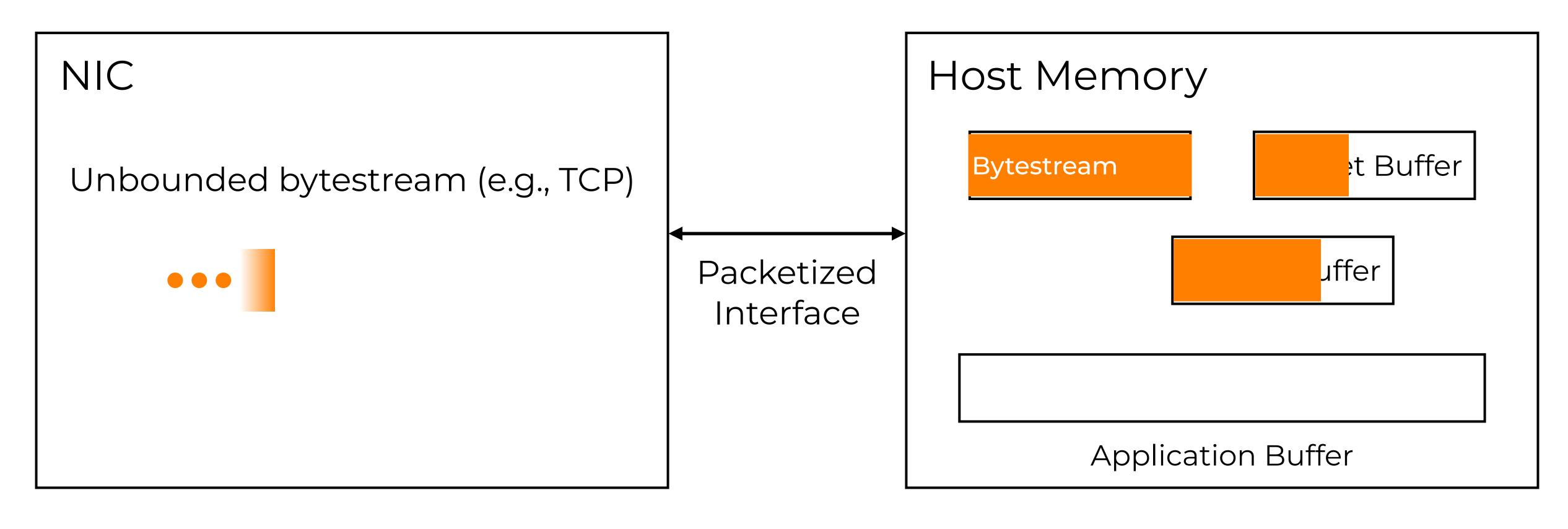


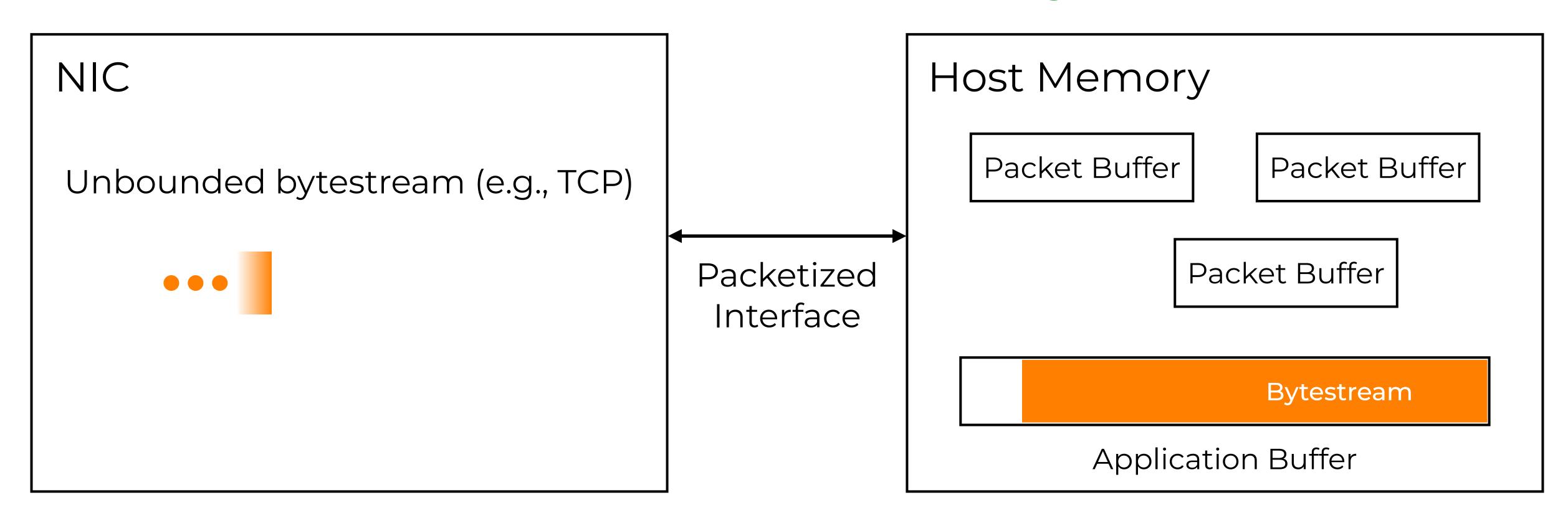




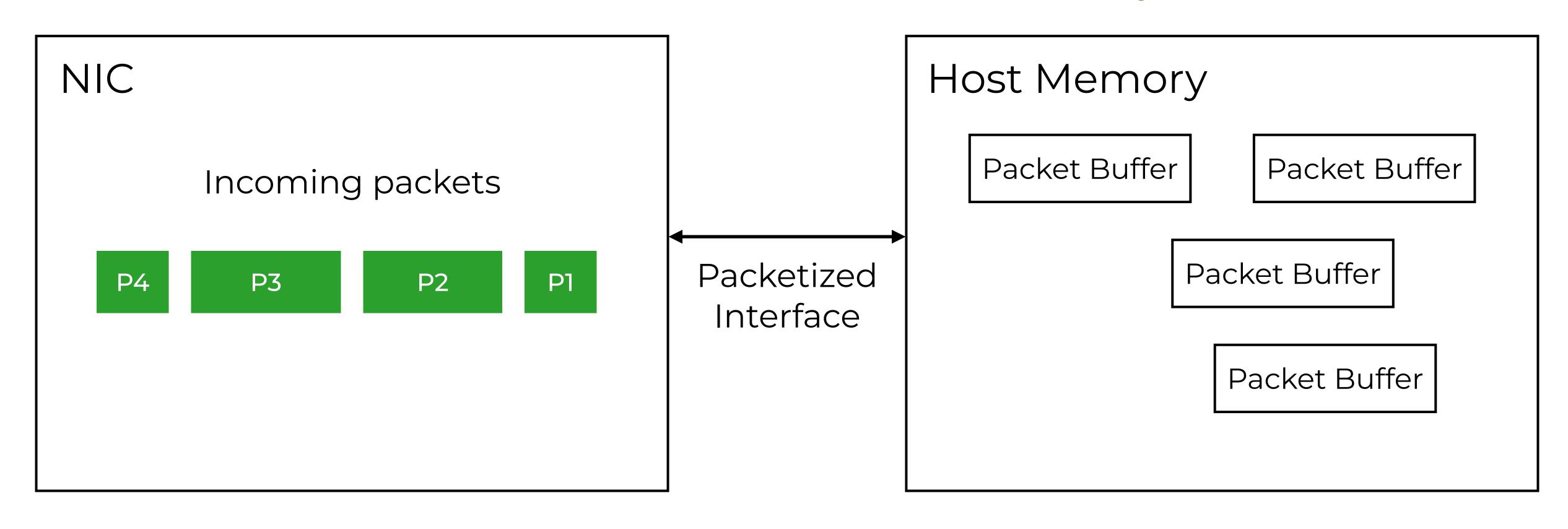




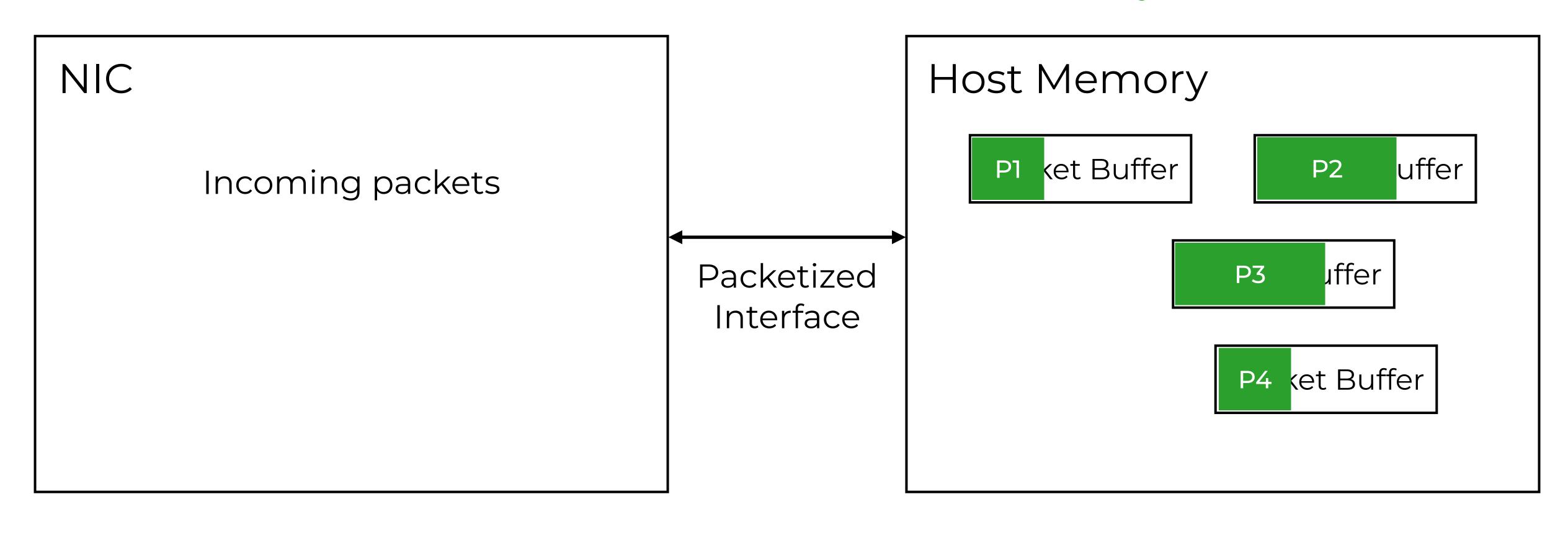




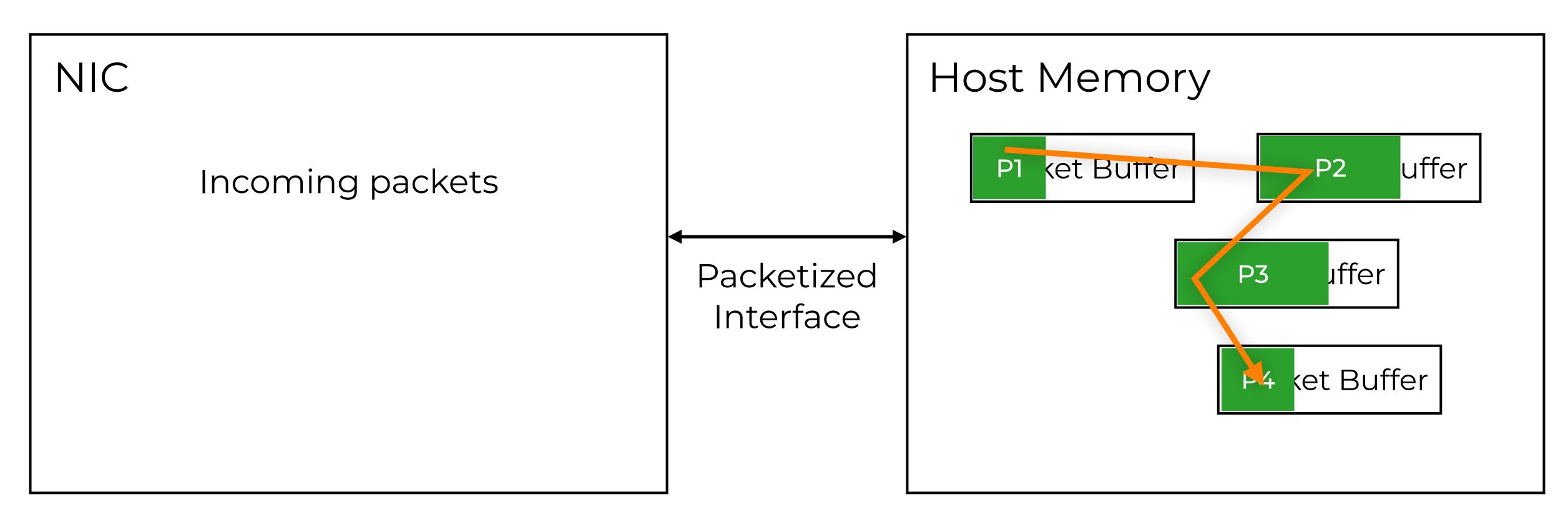
Poor cache interaction due to chaotic memory access



Poor cache interaction due to chaotic memory access



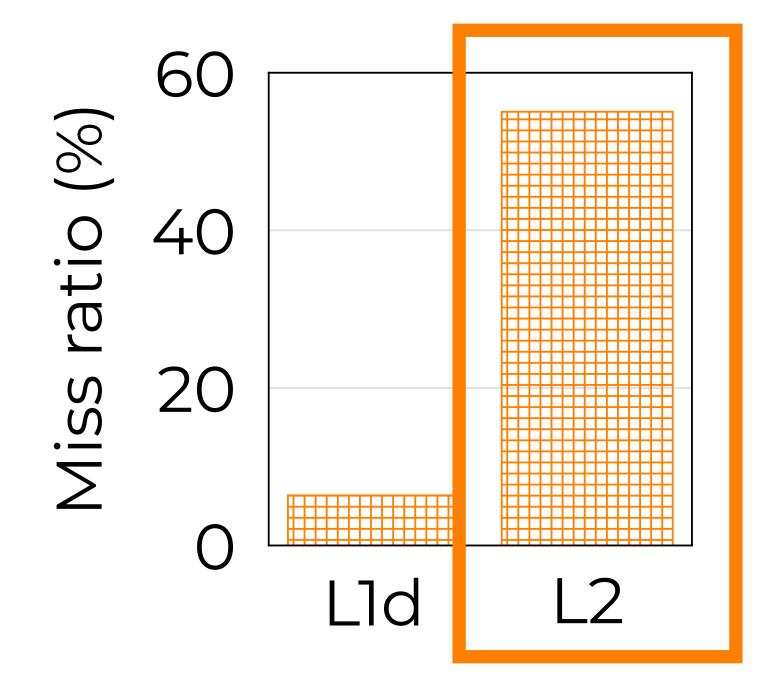
Poor cache interaction due to chaotic memory access

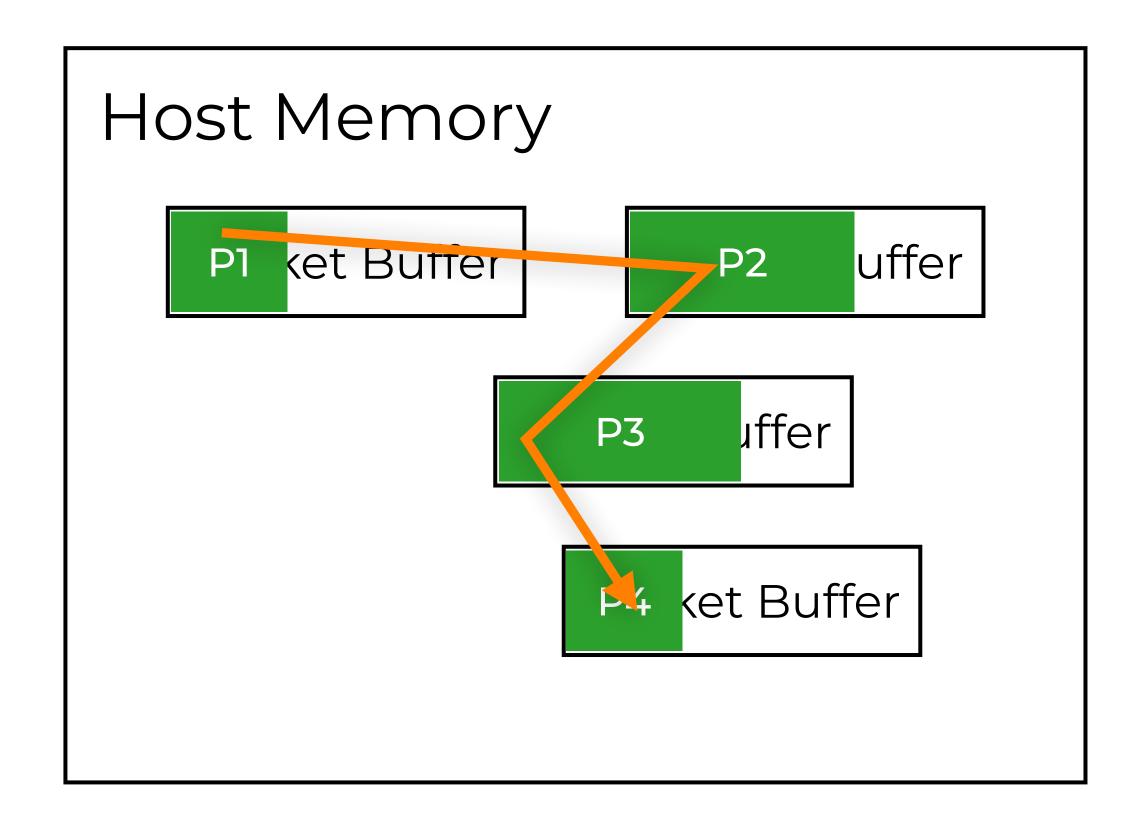


Chaotic Memory Access

Poor cache interaction due to chaotic memory access

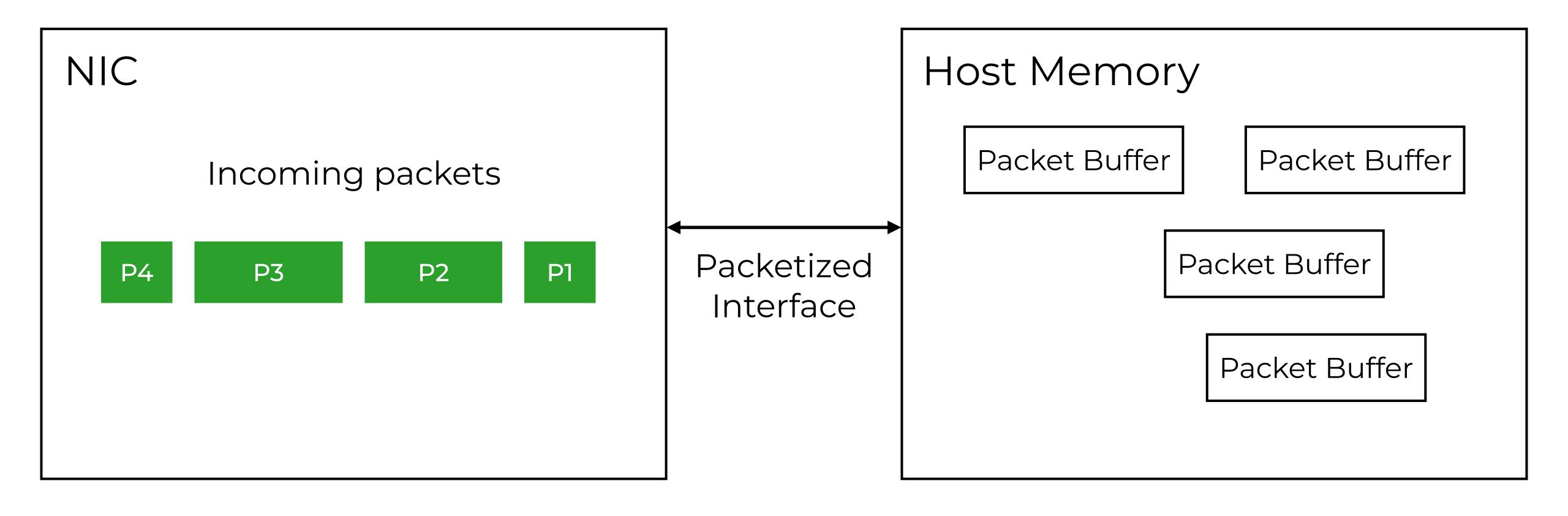
DPDK echo with E810 NIC

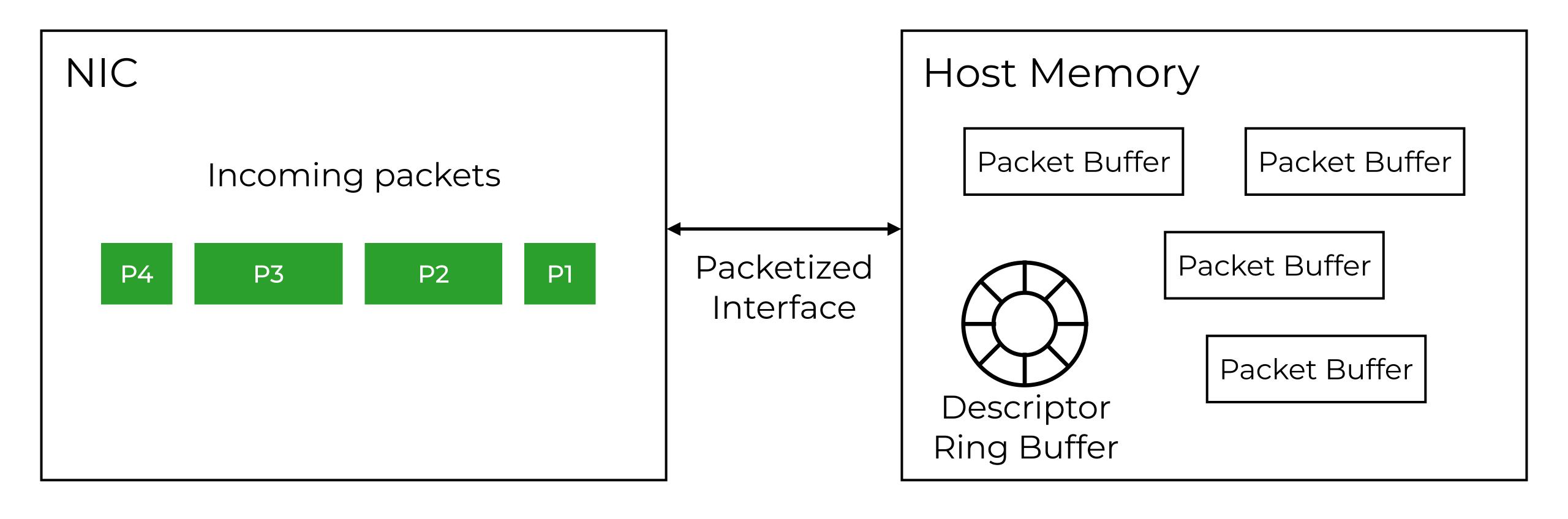


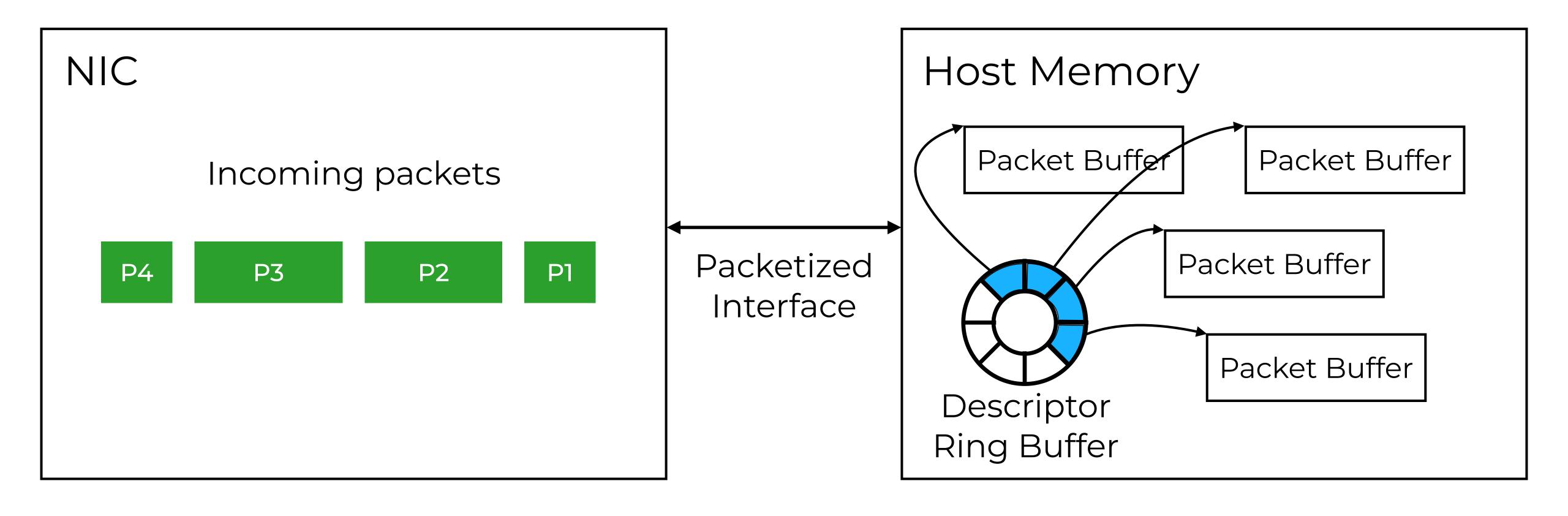


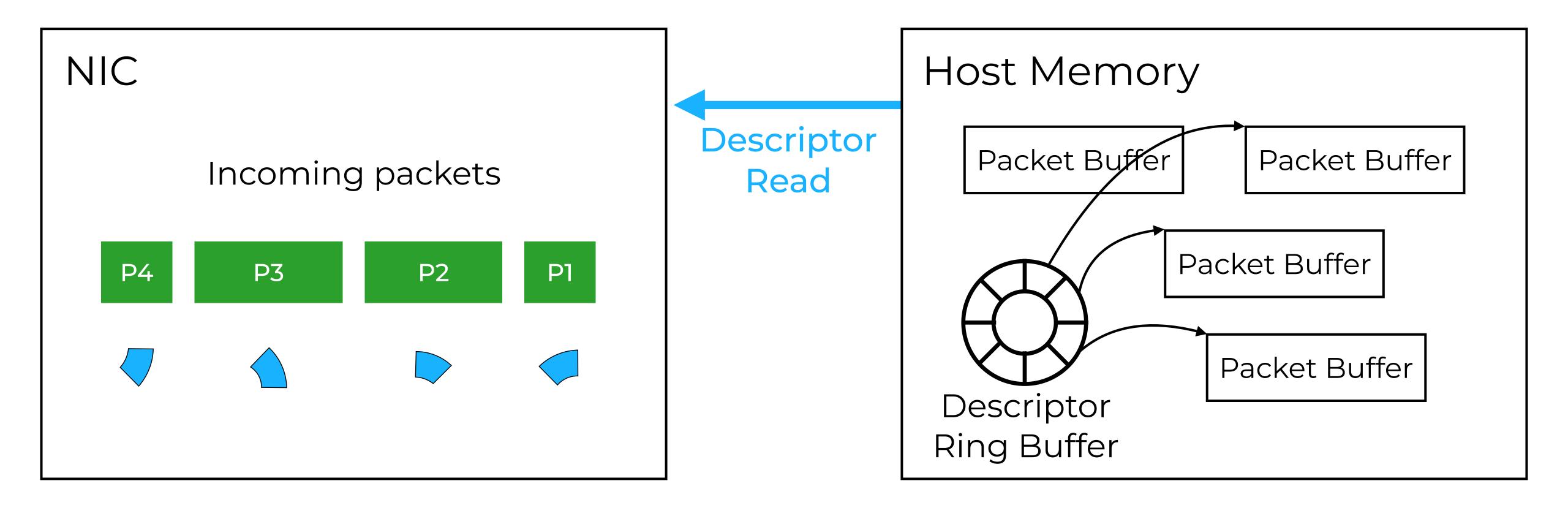
55% Miss Ratio for the L2 Cache

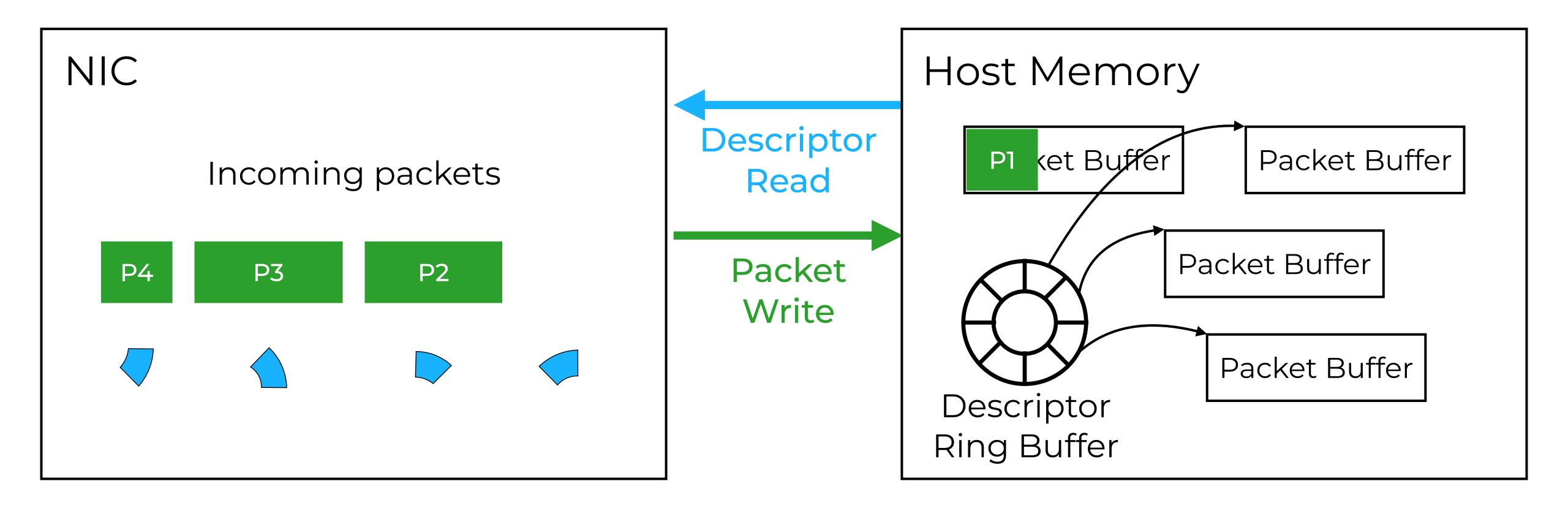
Chaotic Memory Access

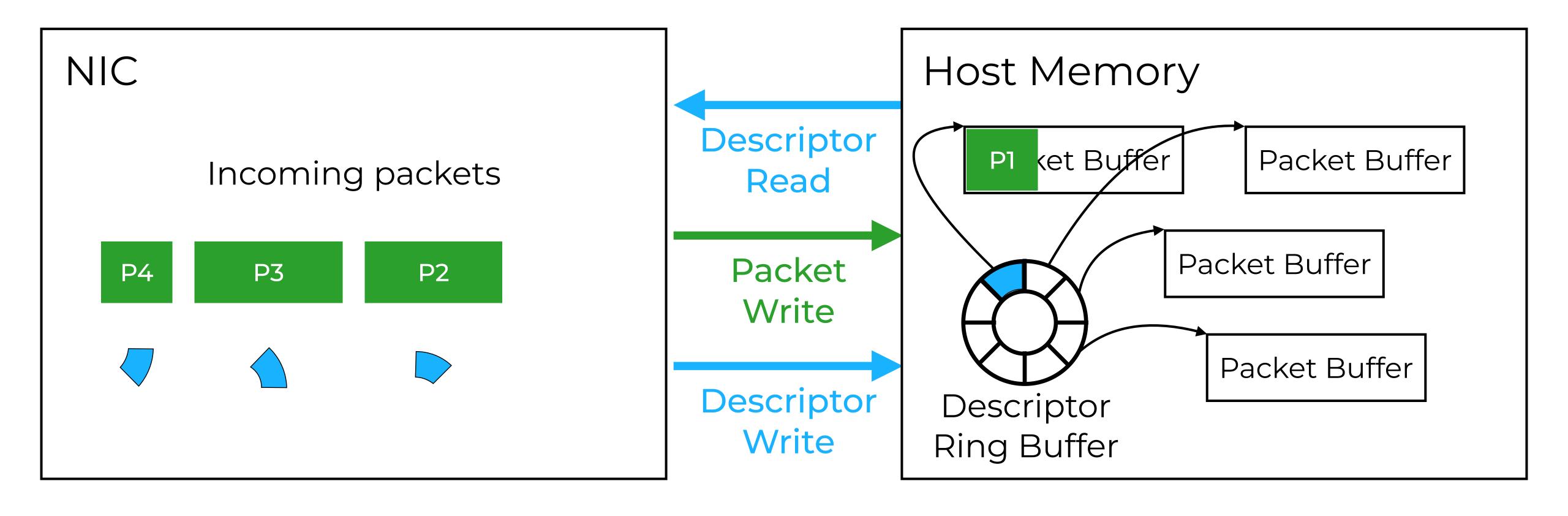












Overhead (PCIe bandwidth and CPU cycles) due to per-packet metadata

DPDK echo with E810 NIC Host Memory PCIe BW (Gbps) 80 Descriptor ket Buffer uffer P2 Read 60 PCIe limit 40 Goodput ıffer P3 Packet 20 Metadata Write P4 ket Buffer RD WR

Descriptor

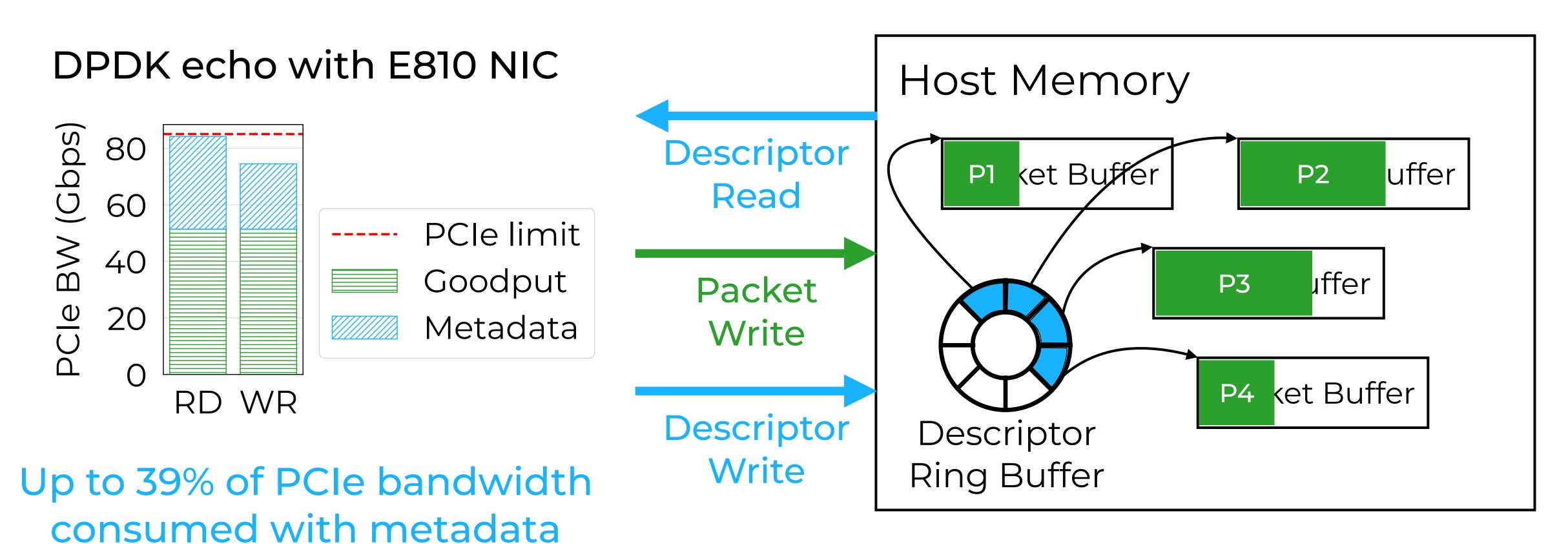
Write

Descriptor

Ring Buffer

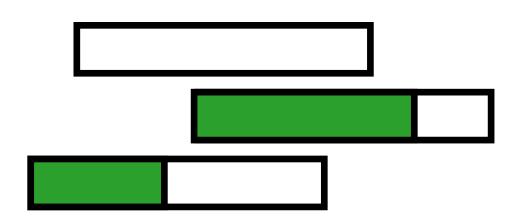
Up to 39% of PCIe bandwidth consumed with metadata

Overhead (PCIe bandwidth and CPU cycles) due to per-packet metadata

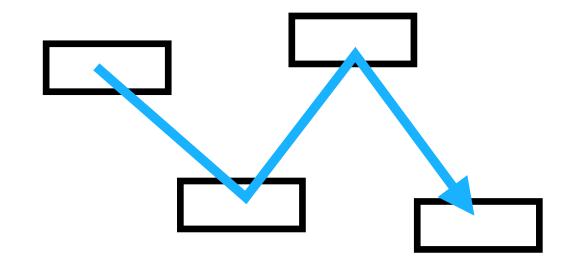


Similar process to transmit packets

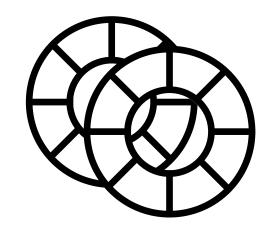
Mismatch between how NICs are used and their interface



#1 Packetized Abstraction



#2 Poor Cache Interaction



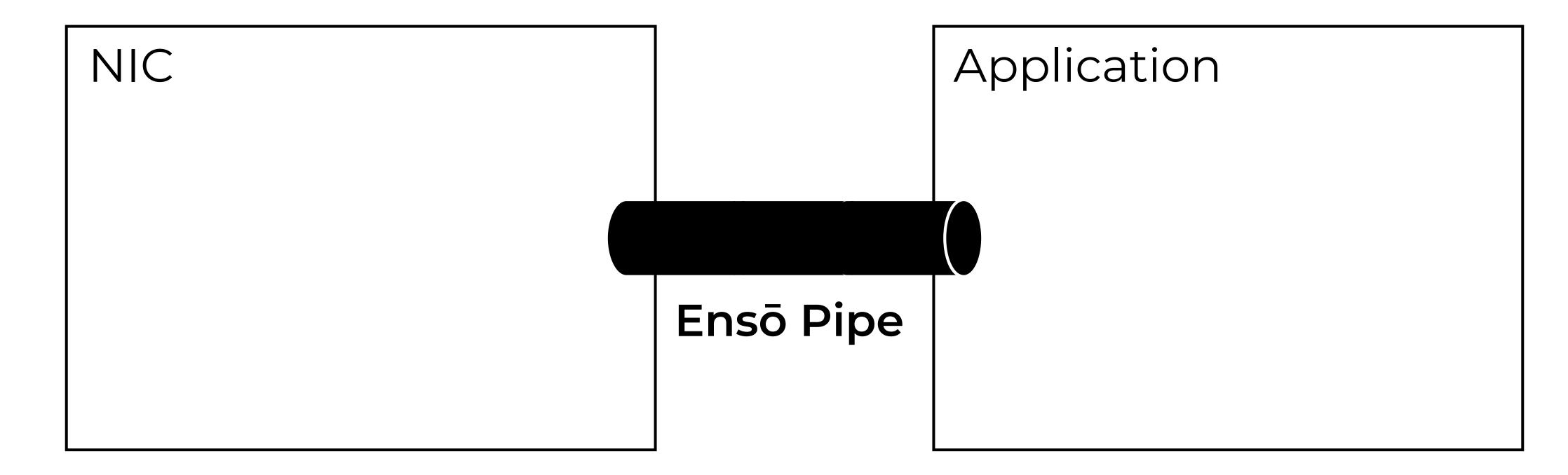
#3 Metadata Overhead

New interface for NIC-Application Communication

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New interface for NIC-Application Communication

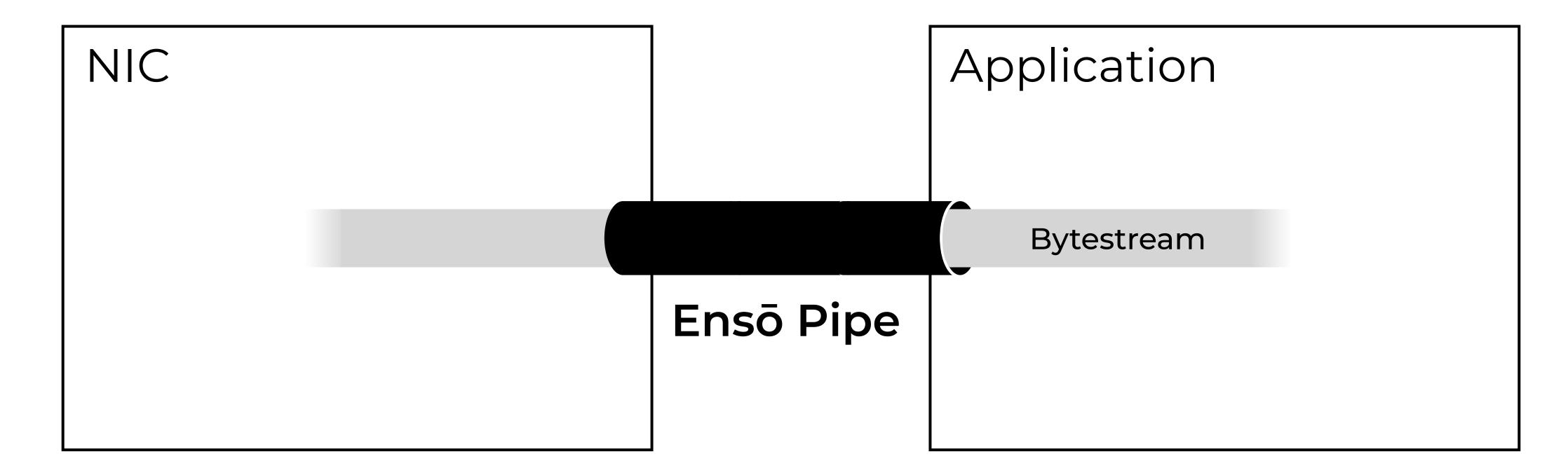
Key Idea: Streaming abstraction



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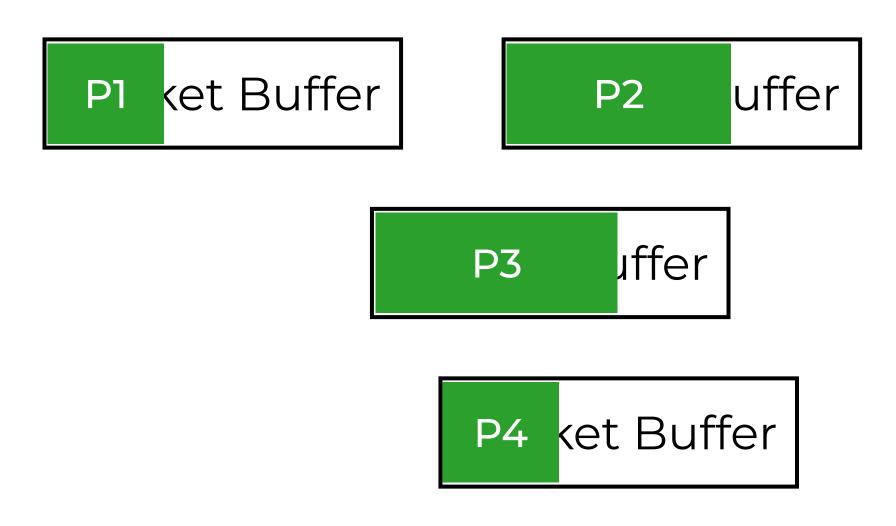
New interface for NIC-Application Communication

Key Idea: Streaming abstraction



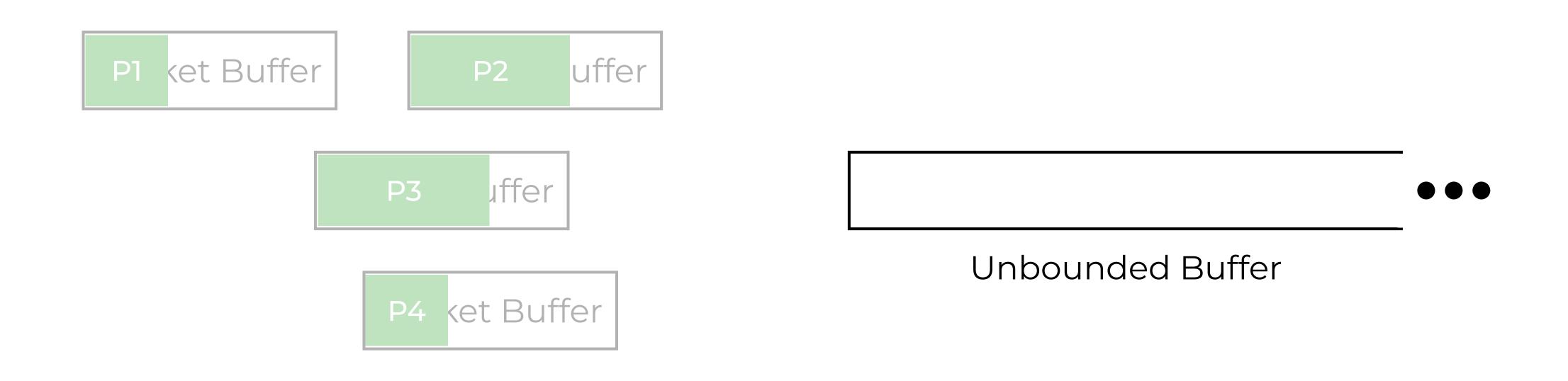
Provide the illusion of an unbounded buffer

Provide the illusion of an unbounded buffer



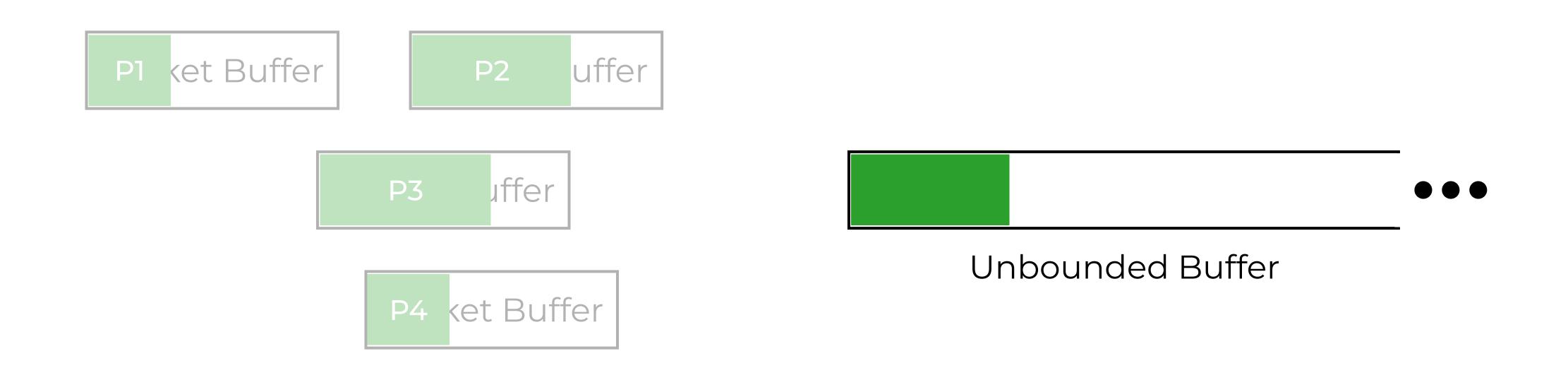
Packetized Abstraction

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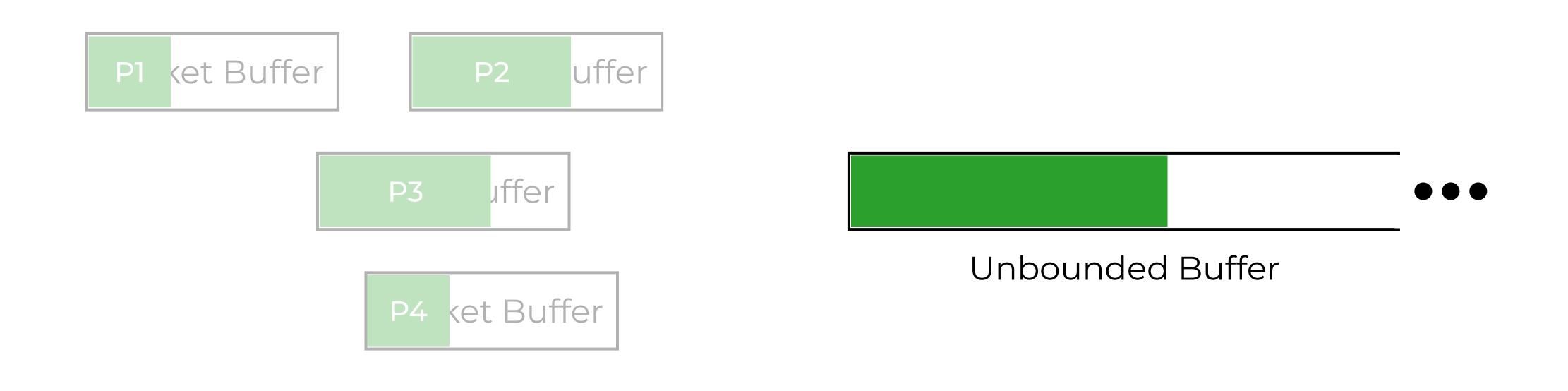
Packetized Abstraction

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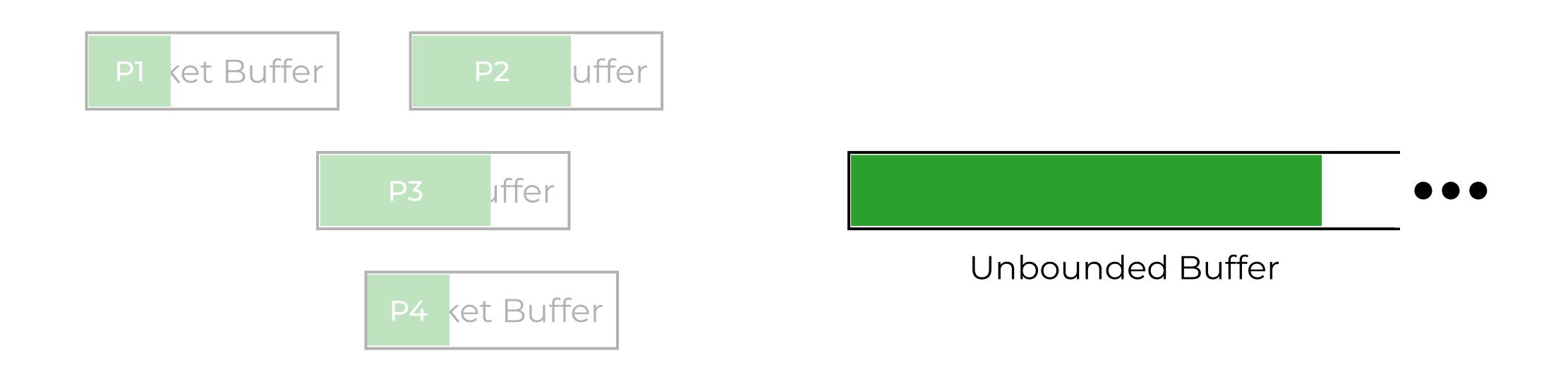
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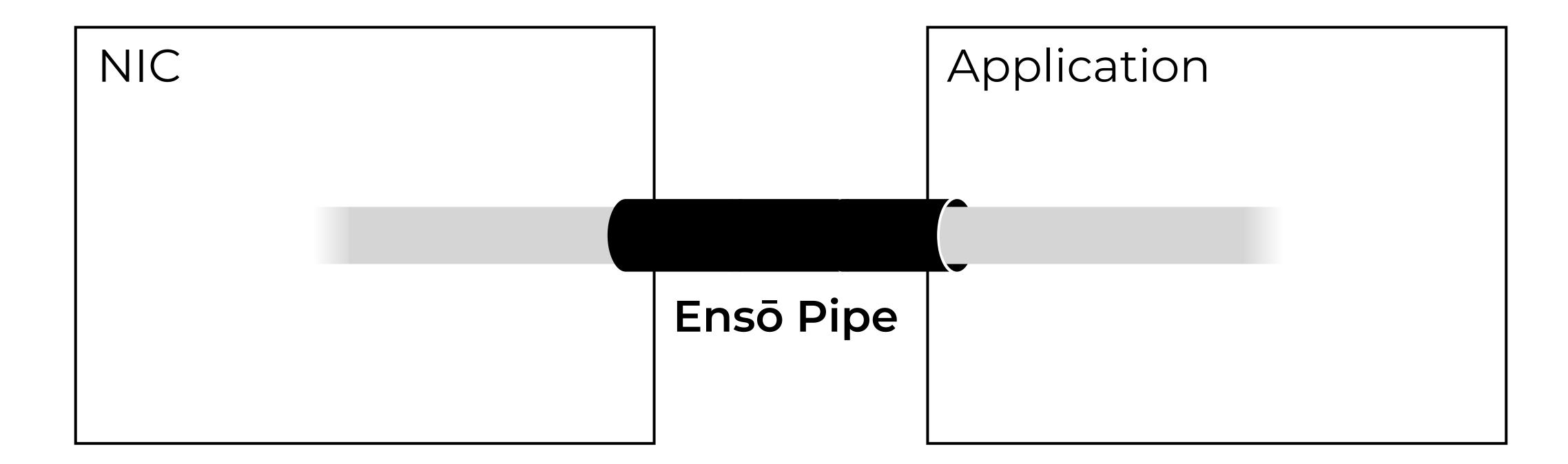
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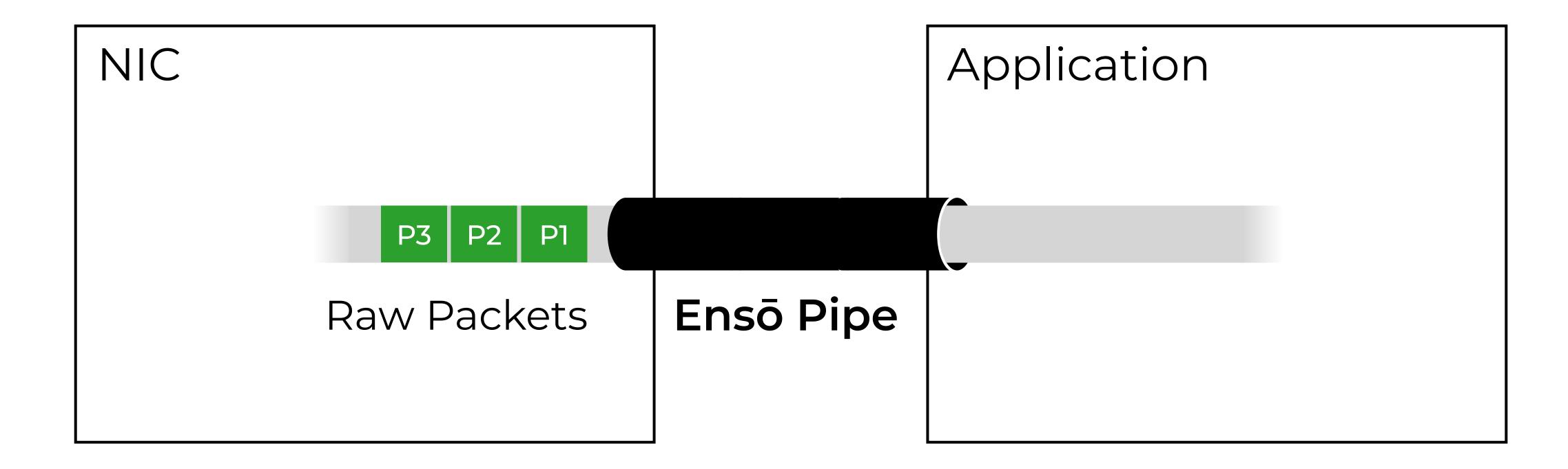


Packetized Abstraction

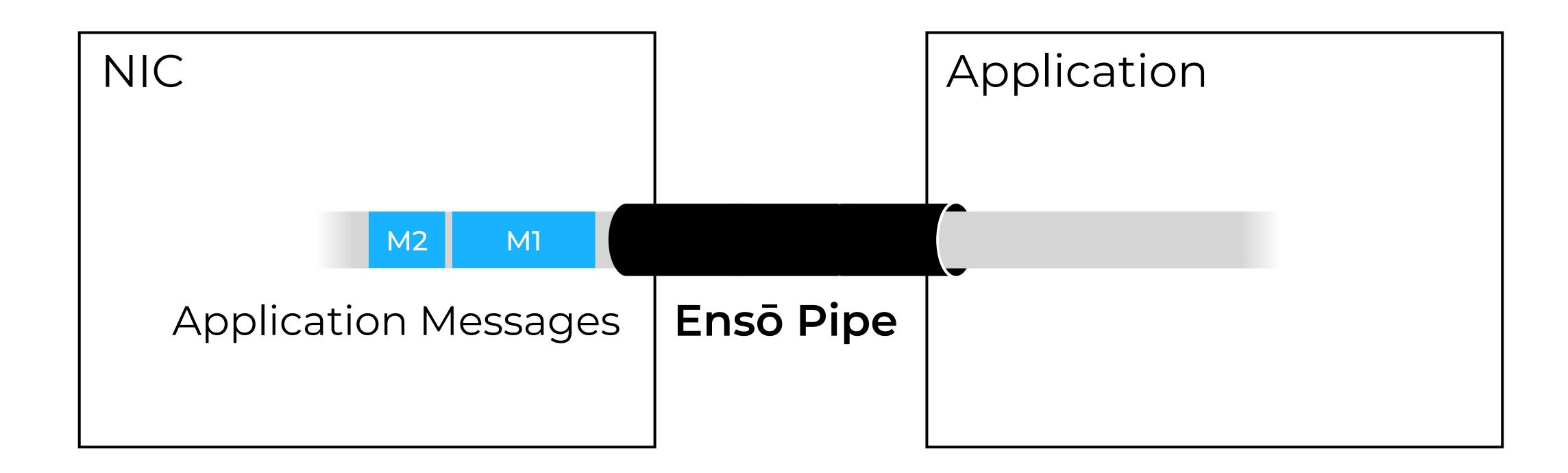
Example 1: NIC with no offloads



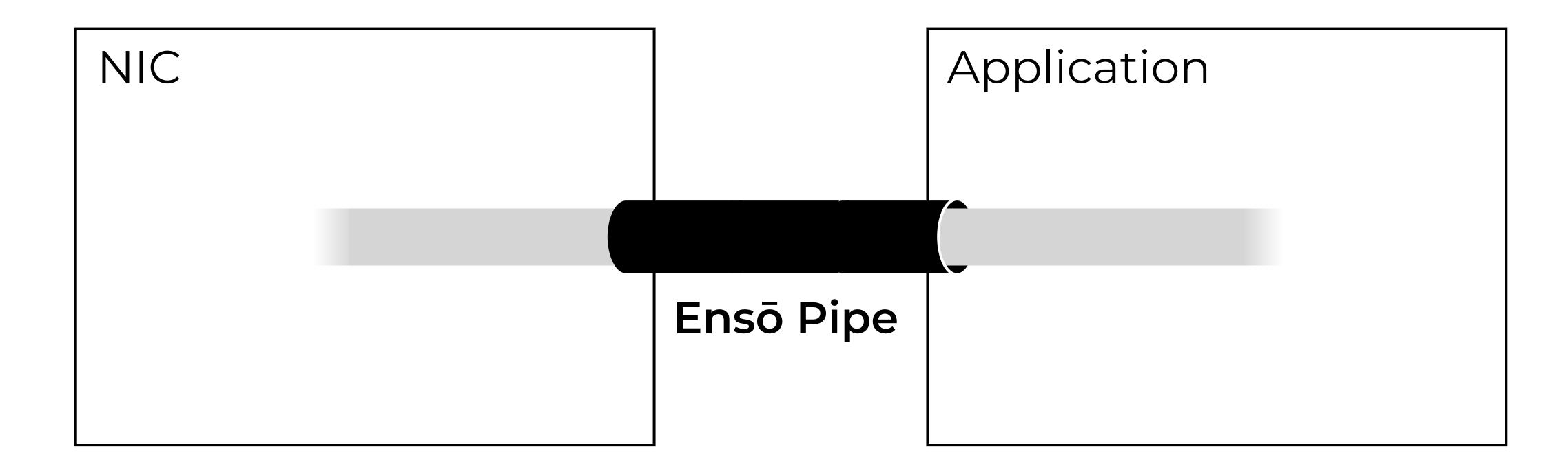
Example 1: NIC with no offloads



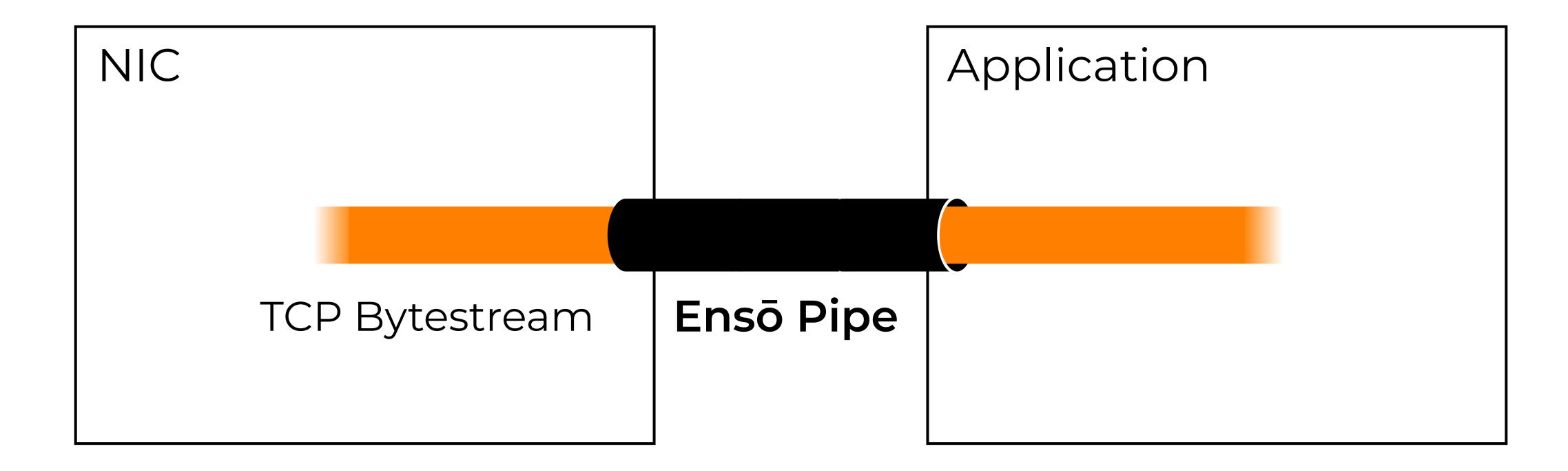
Example 2: NIC that is aware of application-level messages



Example 3: NIC that implements a transport protocol



Example 3: NIC that implements a transport protocol



- 1) How to implement a streaming abstraction?
- 2 How can a streaming abstraction improve performance?

Provide the illusion of an unbounded buffer

Provide the illusion of an unbounded buffer

Ensō Pipe

Each pipe consists of a single contiguous buffer

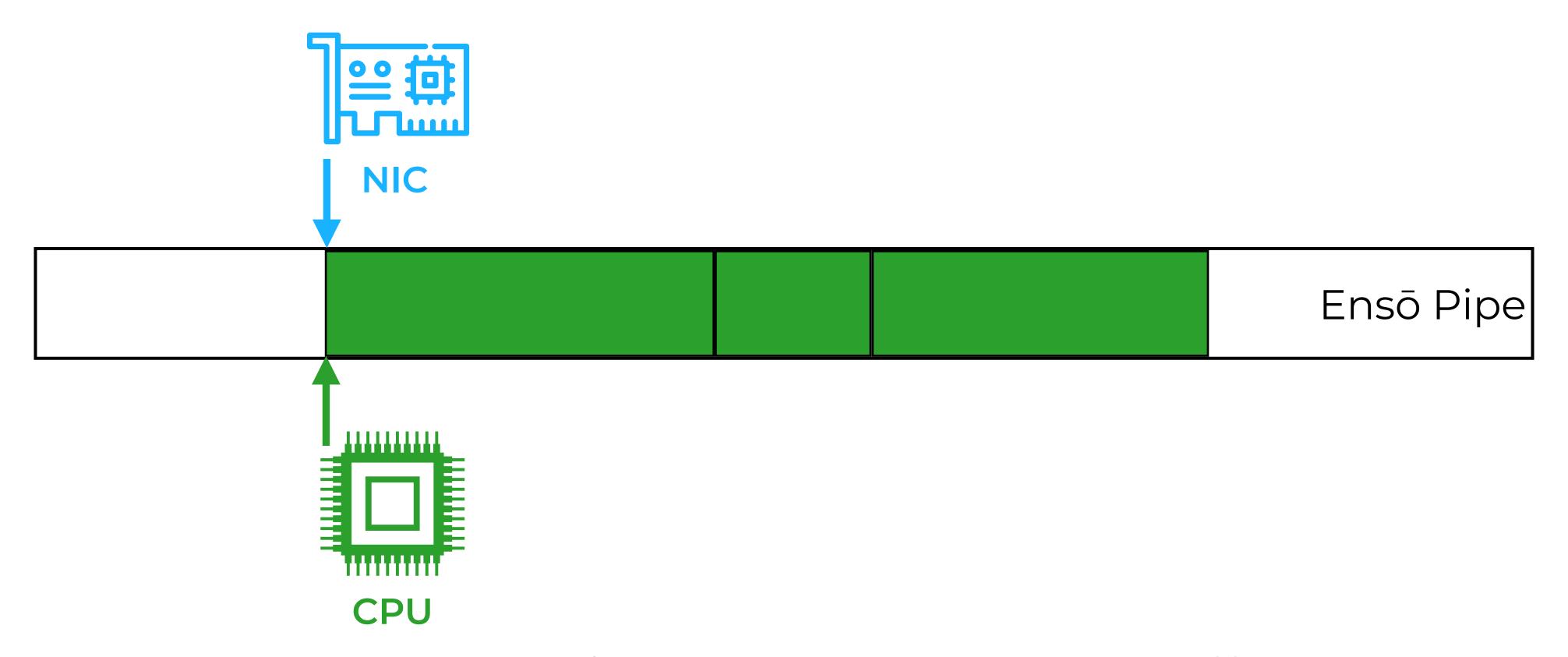
Provide the illusion of an unbounded buffer



Each pipe consists of a single contiguous buffer

We treat this buffer as a ring buffer for data

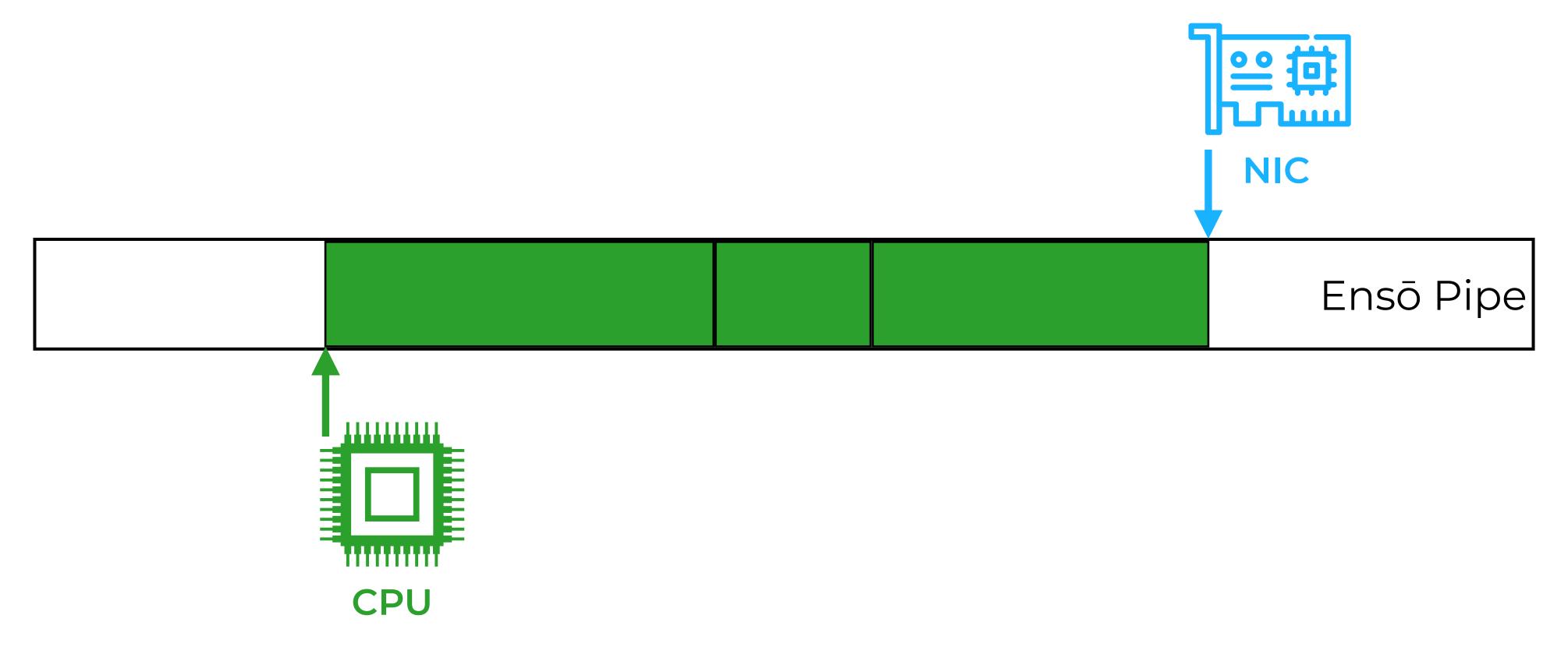
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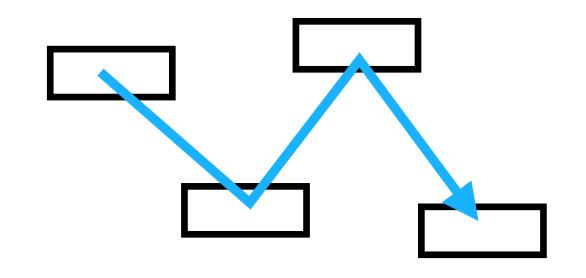


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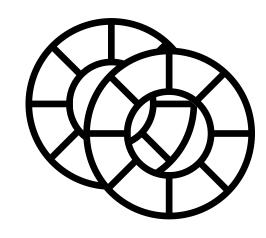
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Packetized Interface

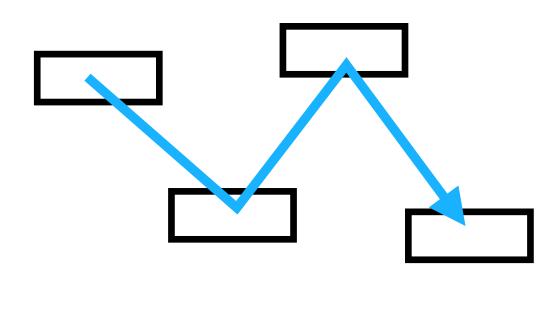


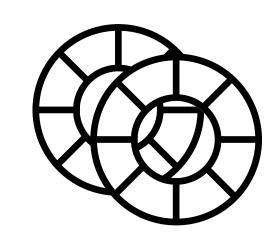
Poor Cache Interaction



Metadata Overhead

Packetized Interface



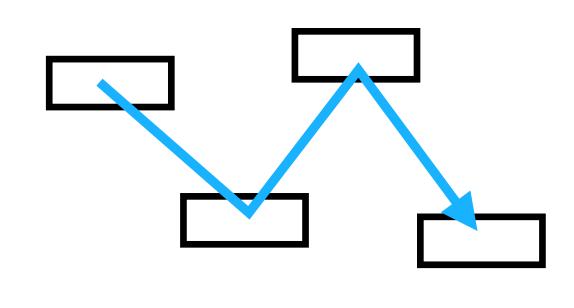


Poor Cache Interaction

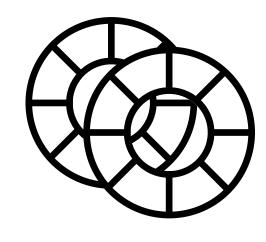
Metadata Overhead

Ensō

Packetized Interface







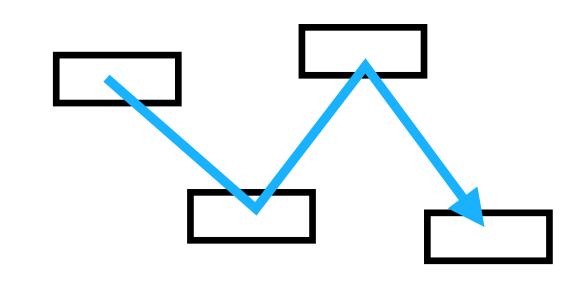
Metadata Overhead

Ensō

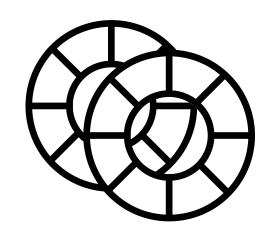


Sequential Memory Access

Packetized Interface







Metadata Overhead

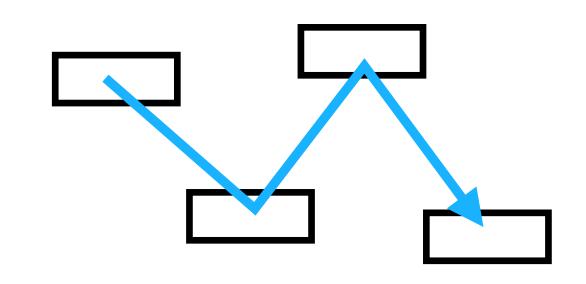
Ensō



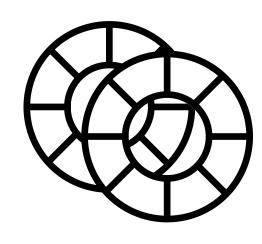
Sequential Memory Access

Reduces L1 misses by 95.9% and L2 misses by 99.5%

Packetized Interface



Poor Cache Interaction



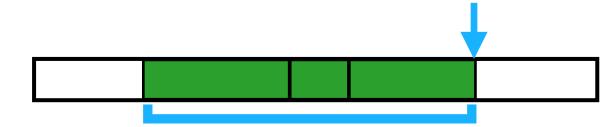
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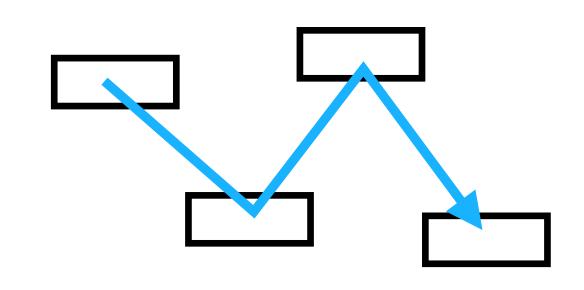
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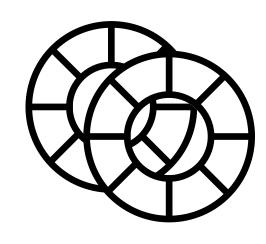


Notifying Batches

Packetized Interface

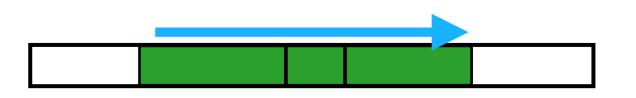


Poor Cache Interaction



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Notifying Batches

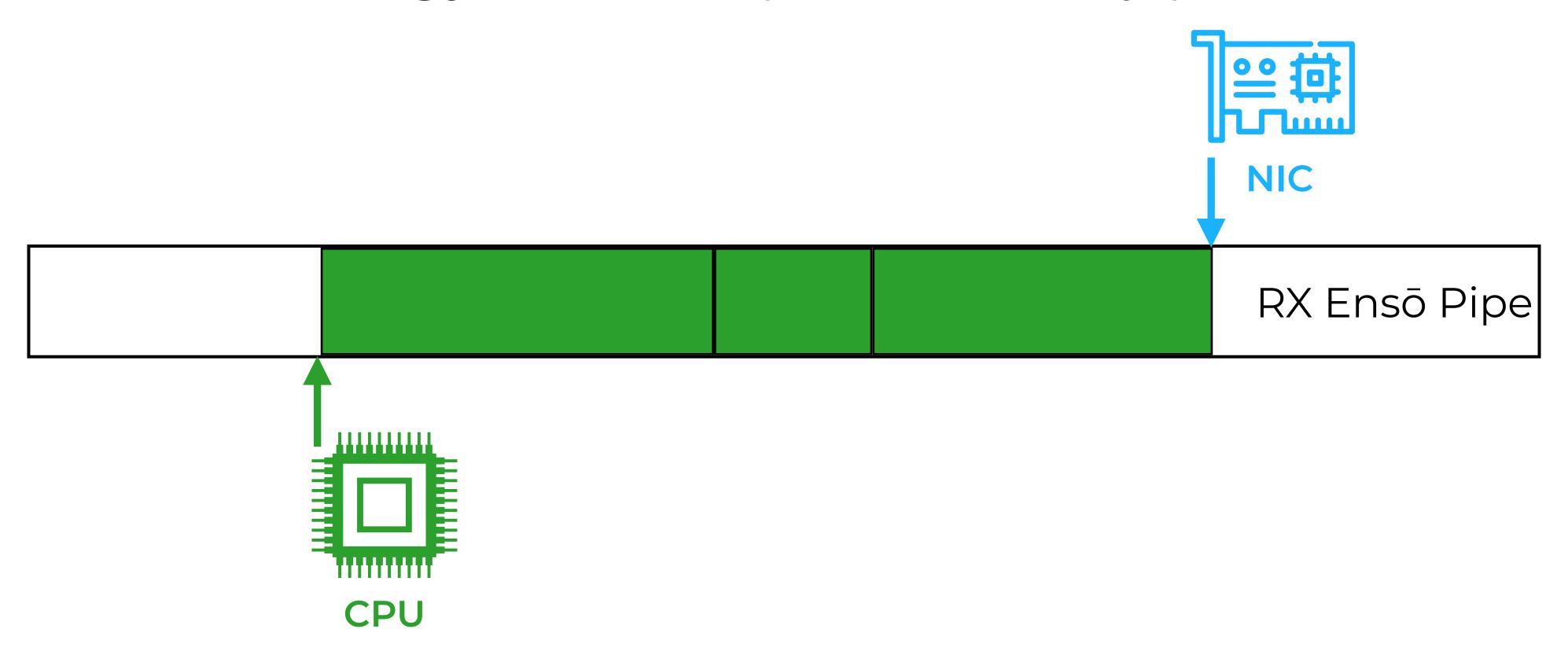
Reduces PCIe metadata traffic by 96.9%

RX Ensō Pipe

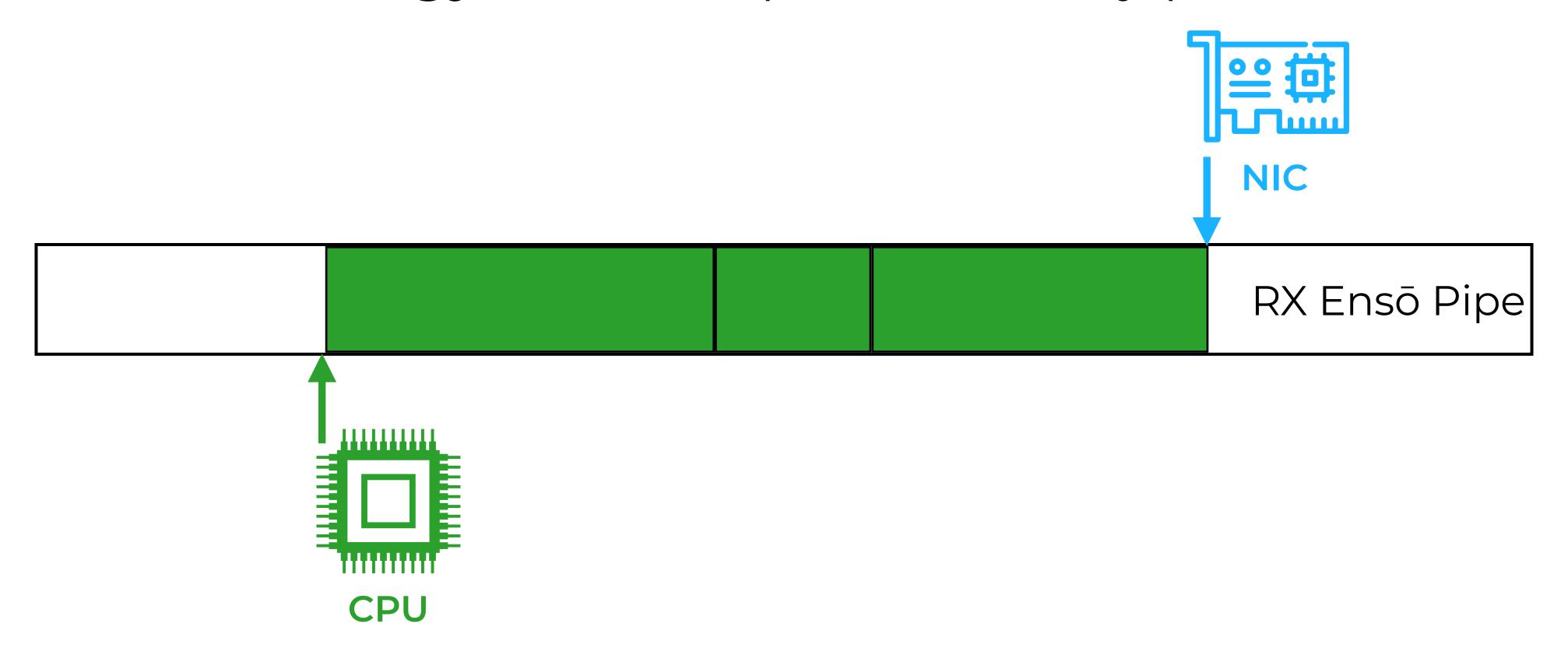
Naïve strategy: send an update for every piece of data



Naïve strategy: send an update for every piece of data



Naïve strategy: send an update for every piece of data



Problem: Per-packet overhead

Notification Pacing in Ensō

Ensō combines two techniques

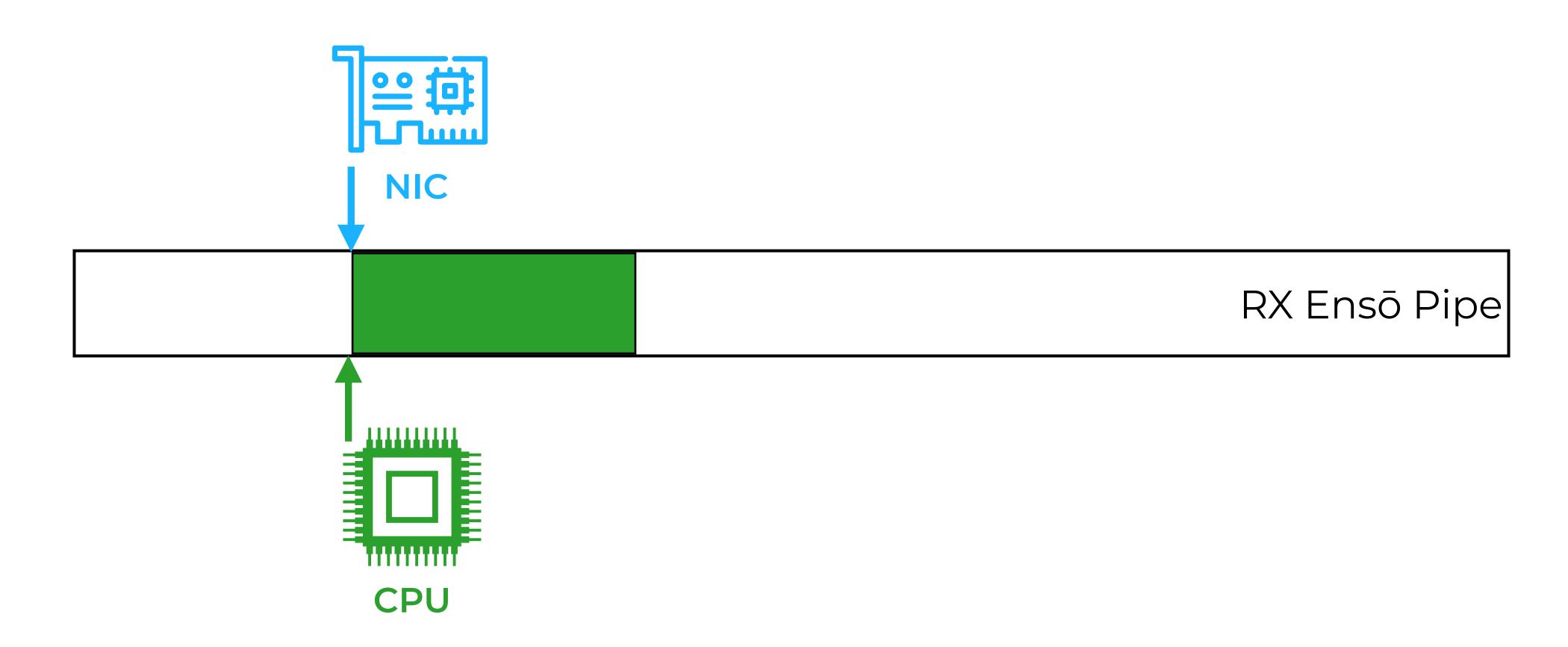


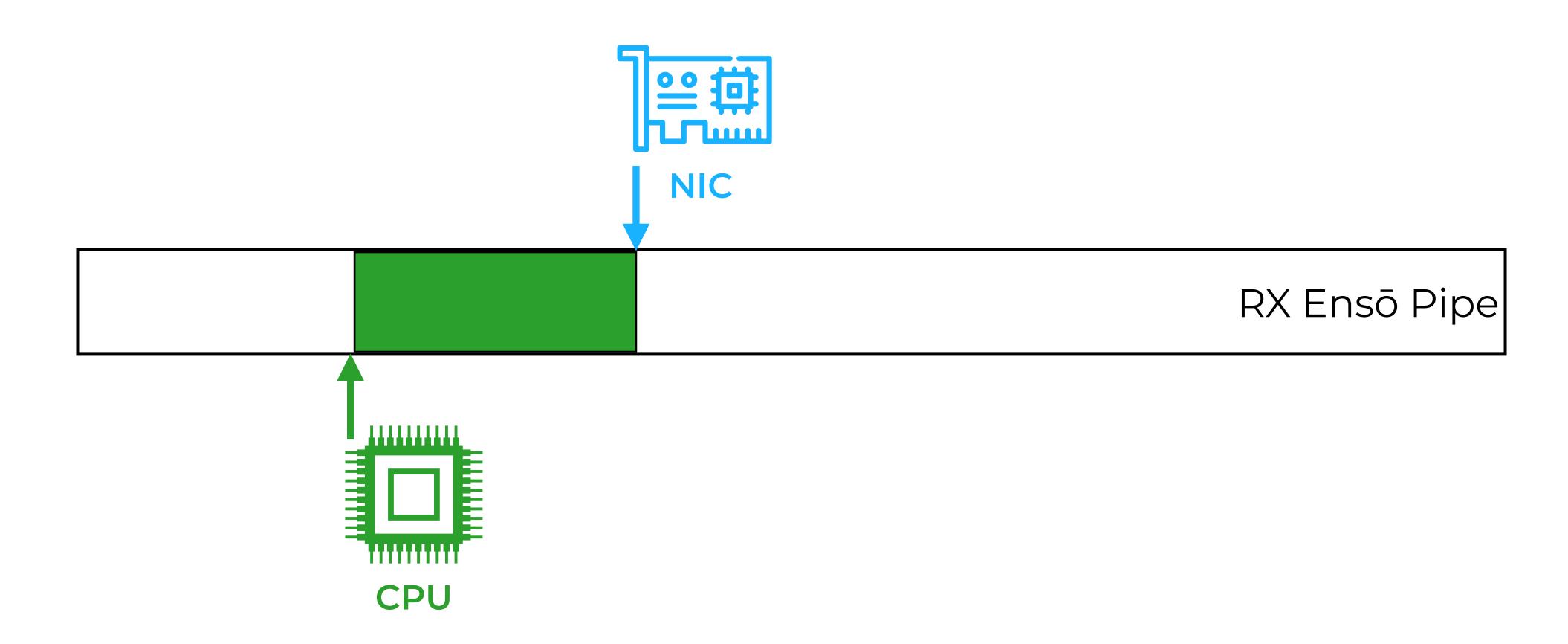
1) Reactive Notifications

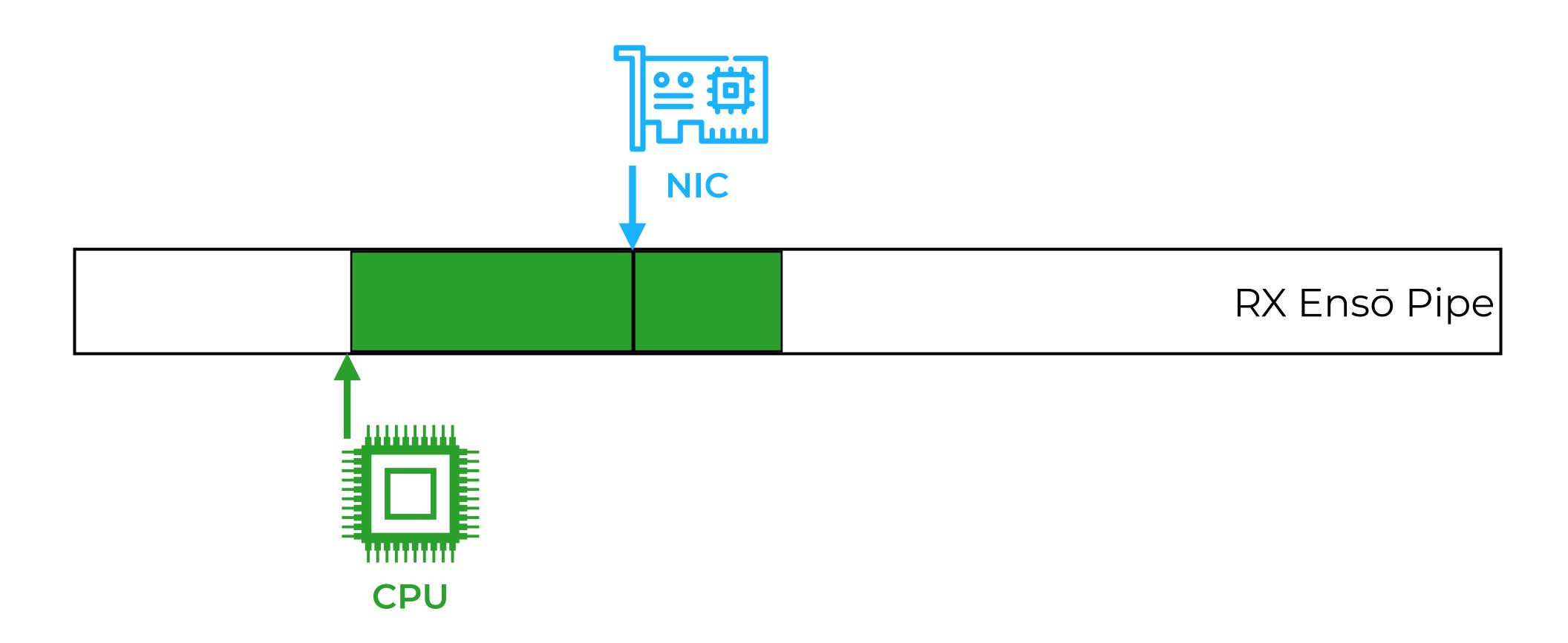


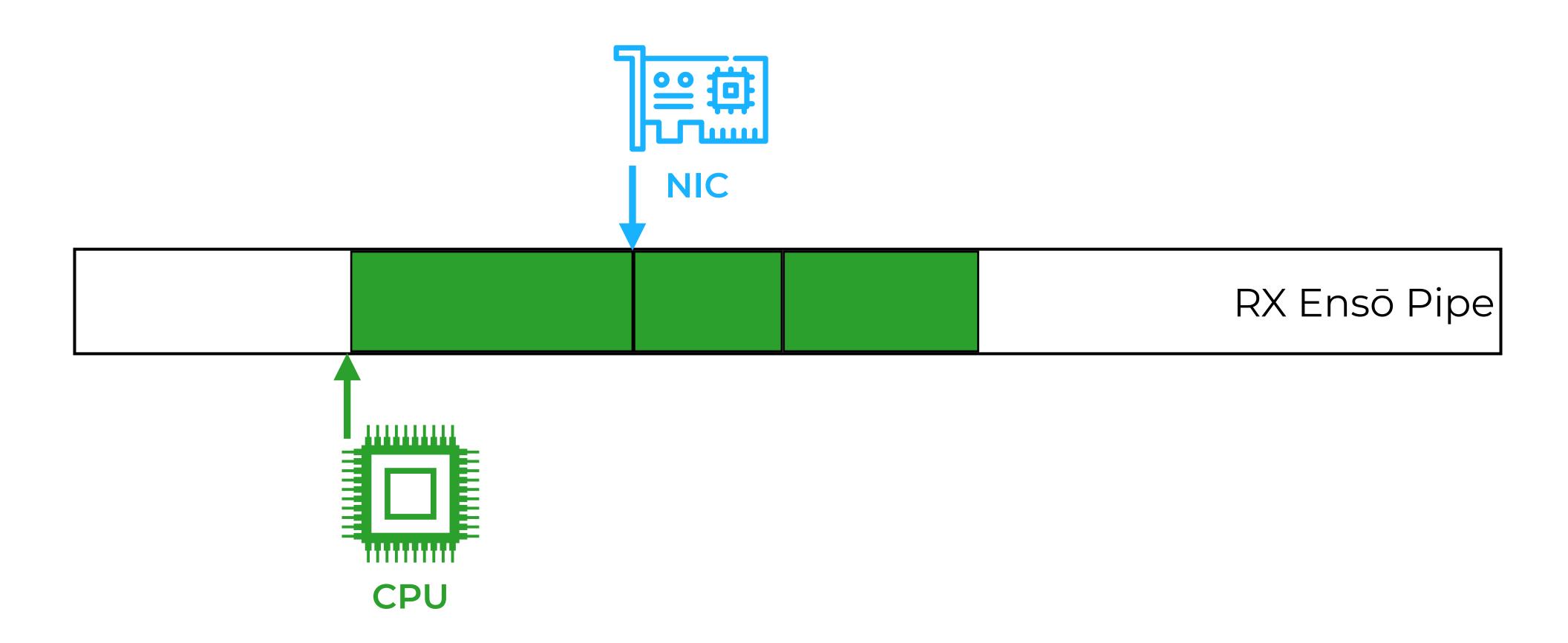
2 Notification Prefetching

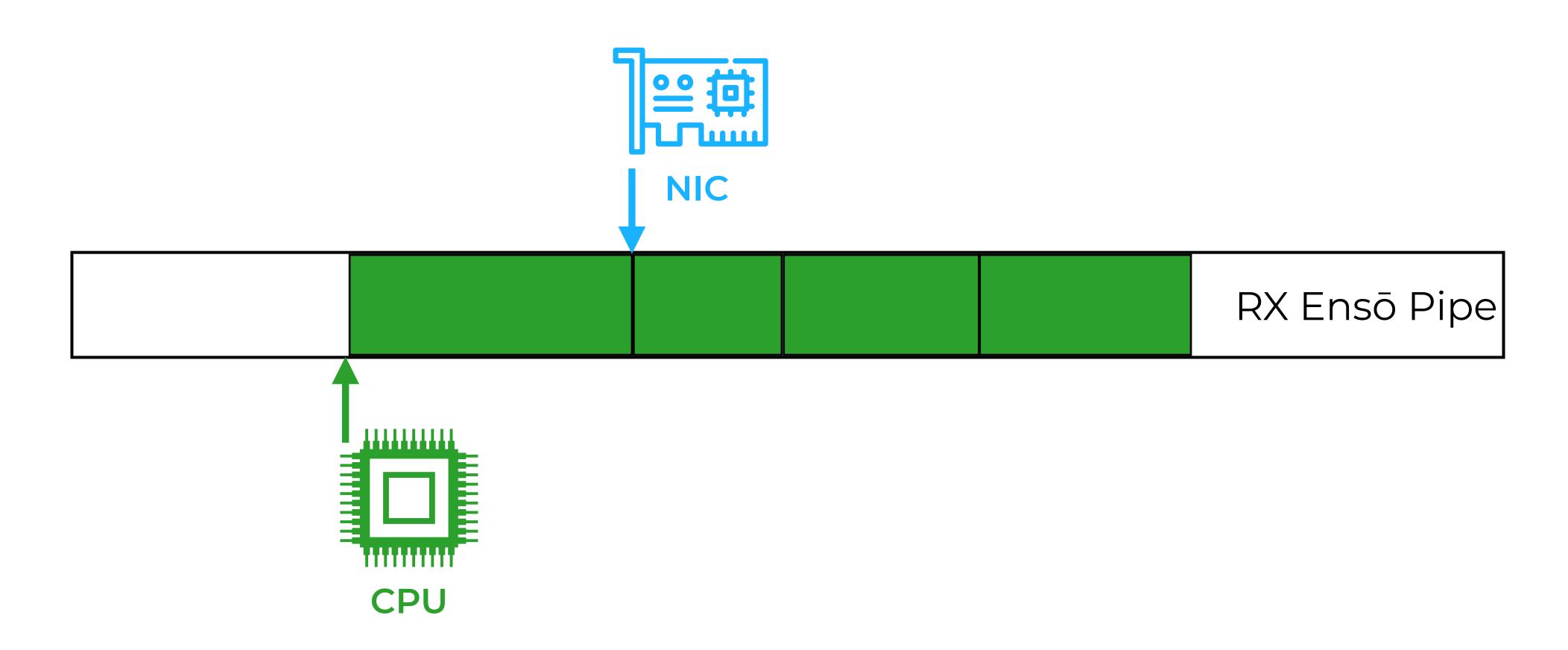


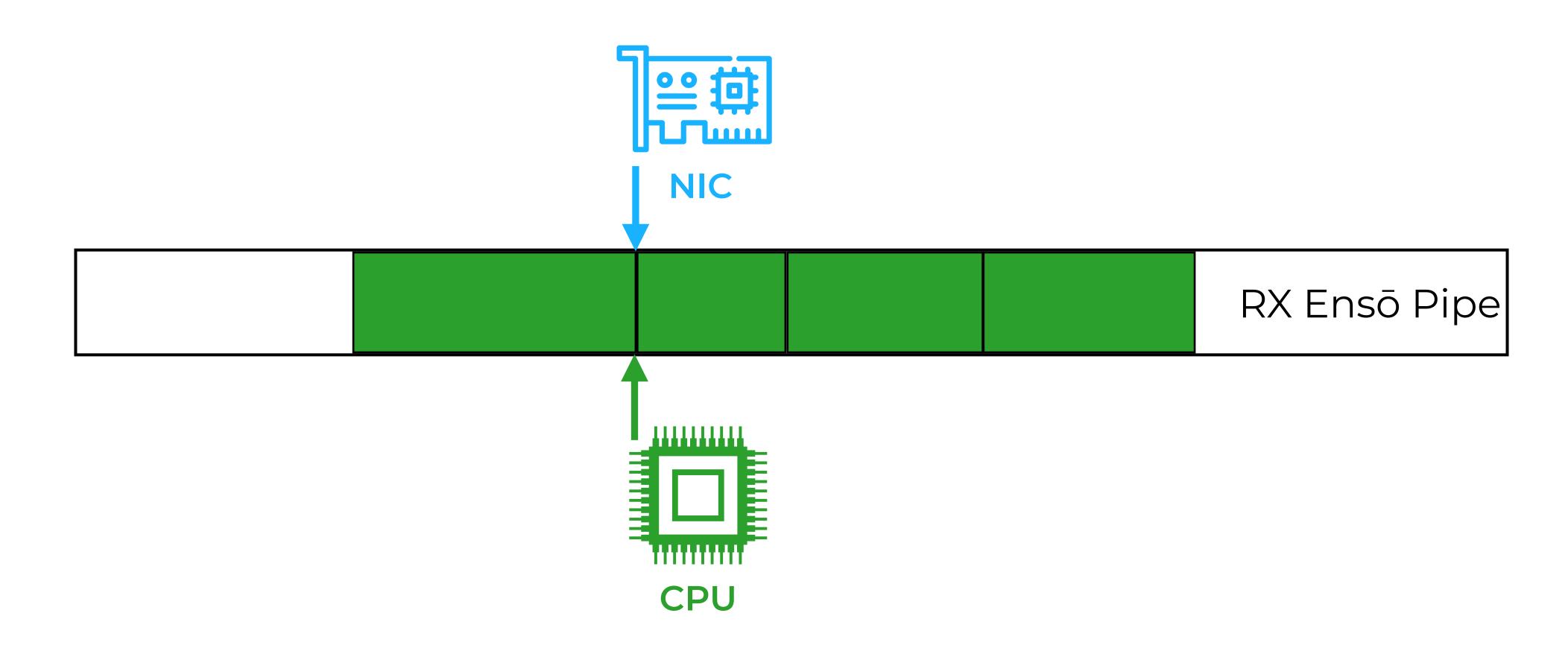


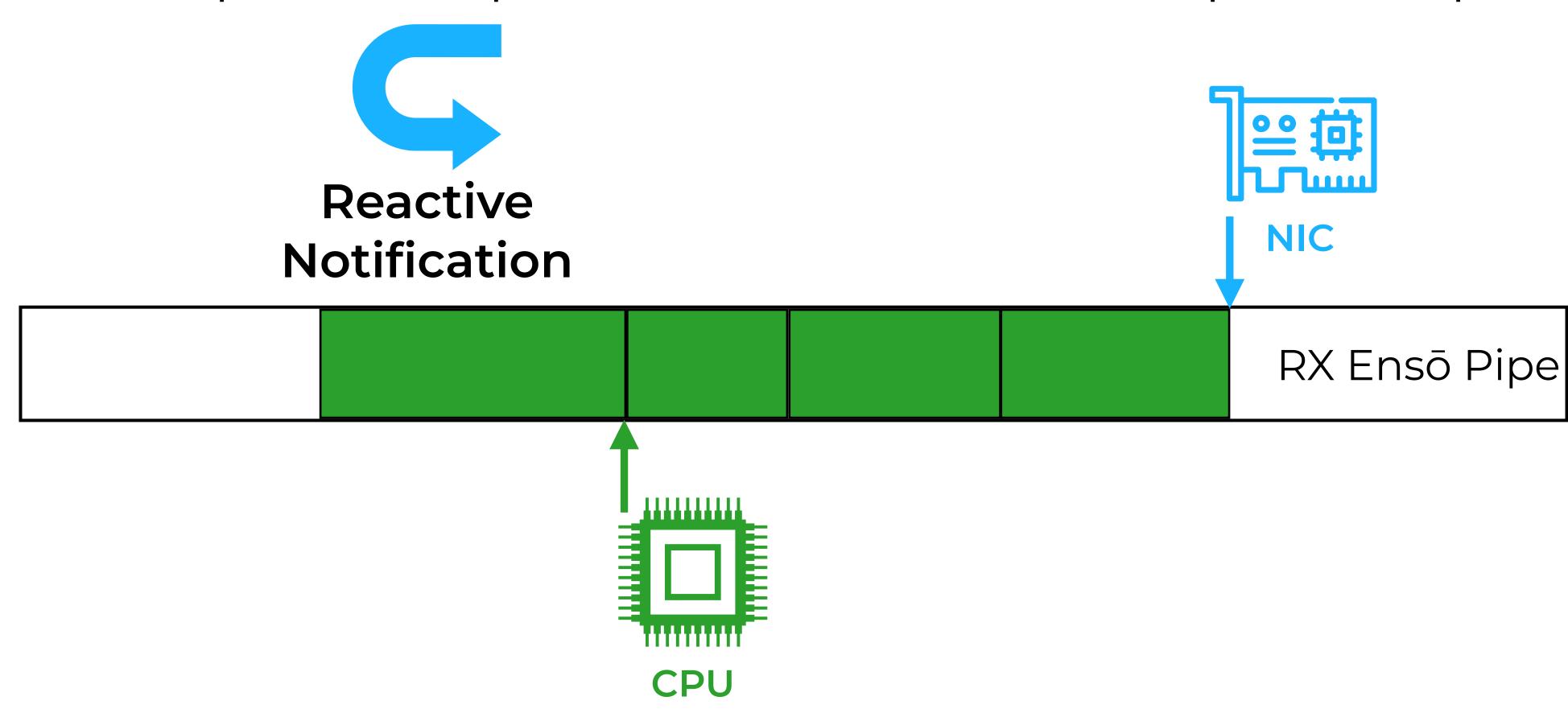




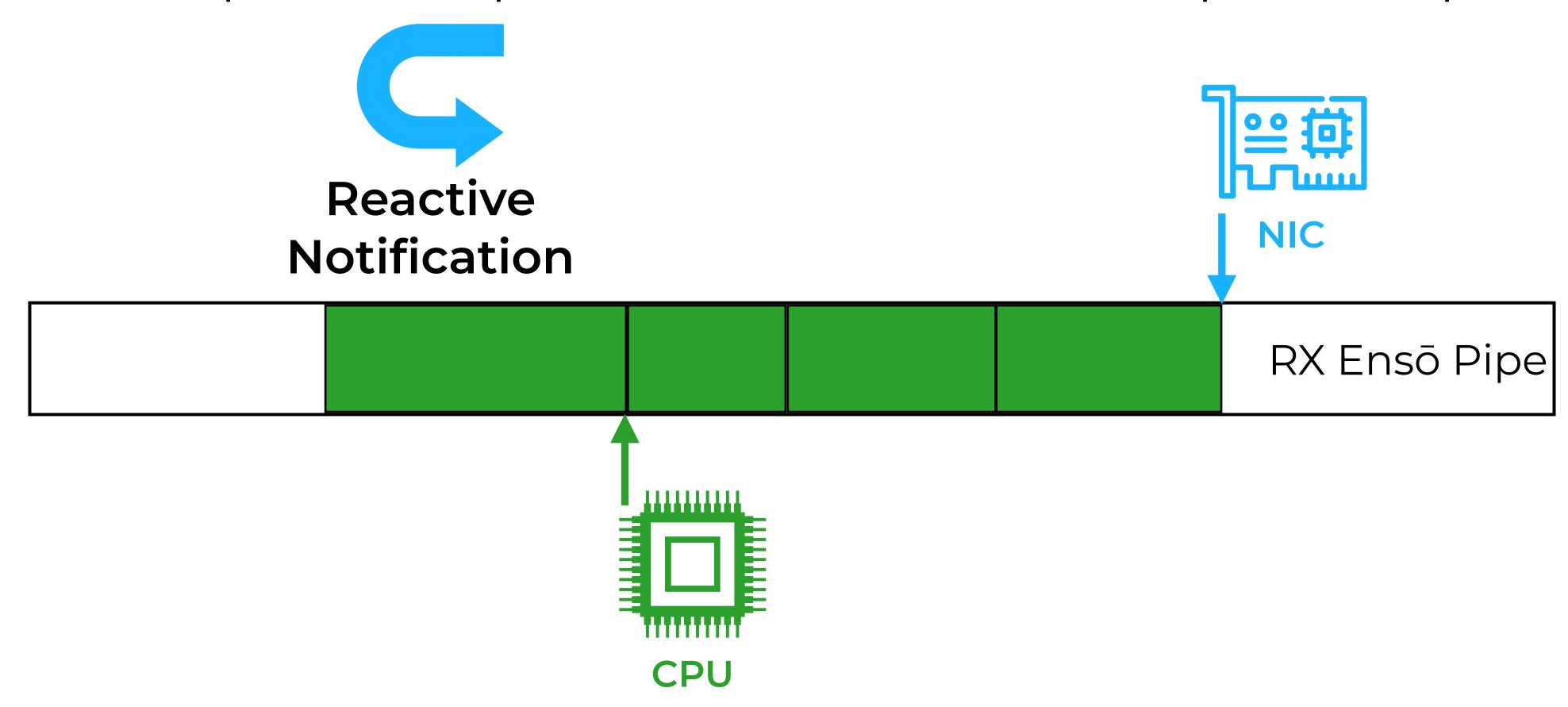




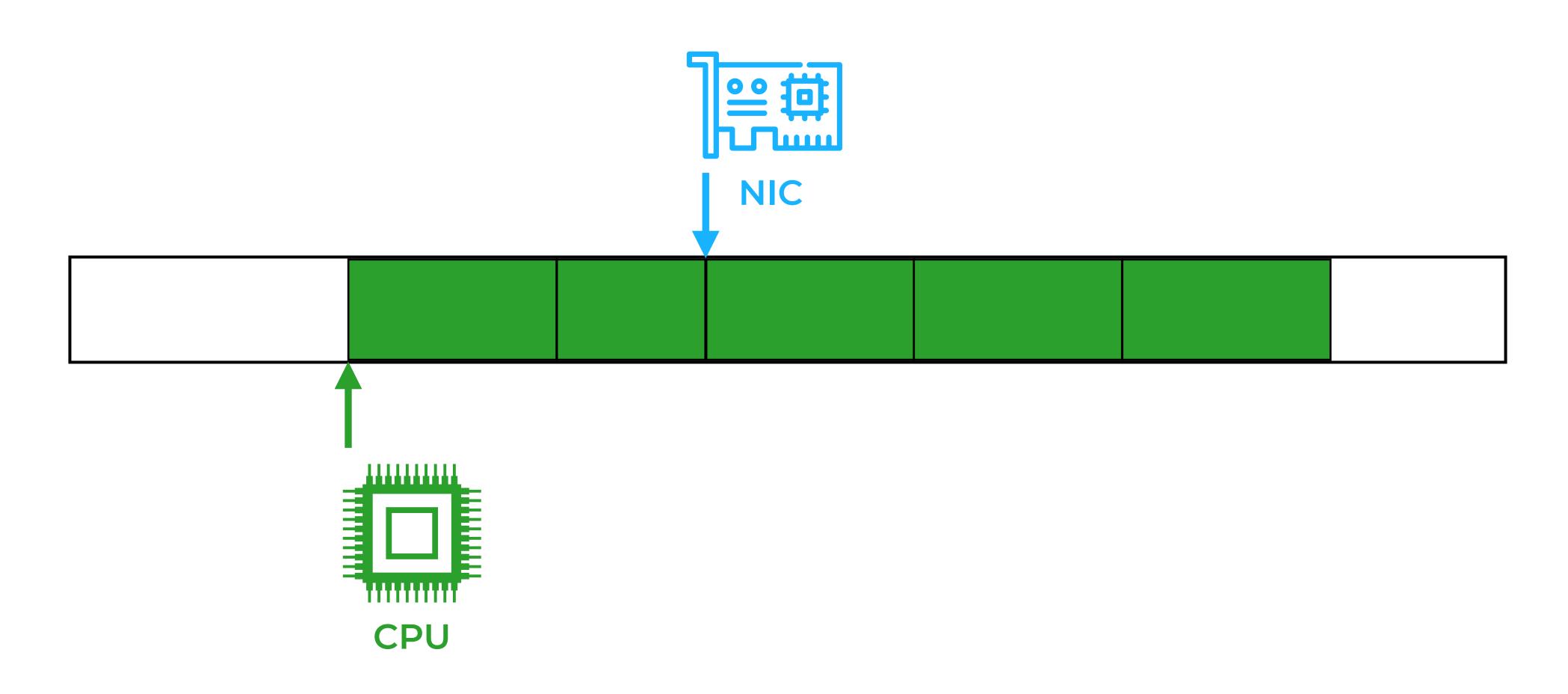


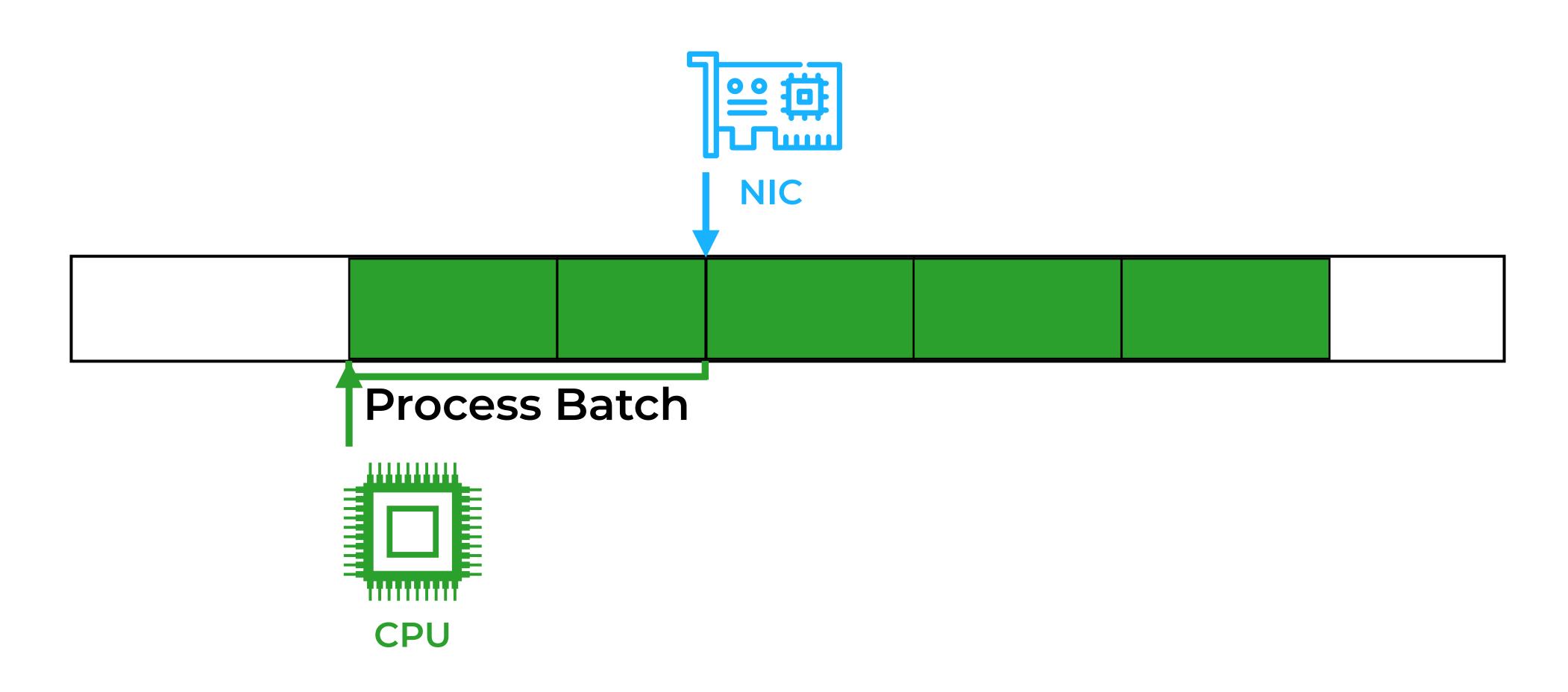


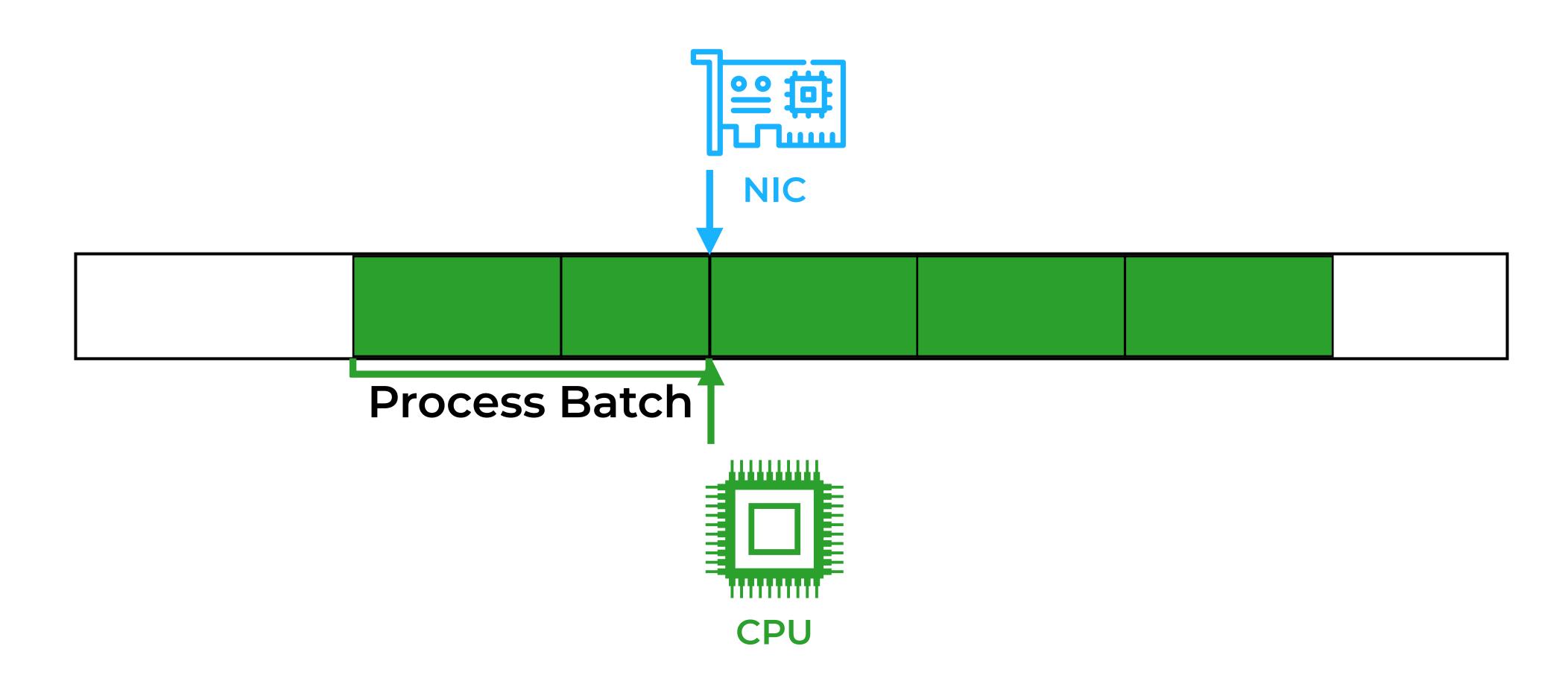
The NIC updates its pointer in reaction to CPU pointer updates

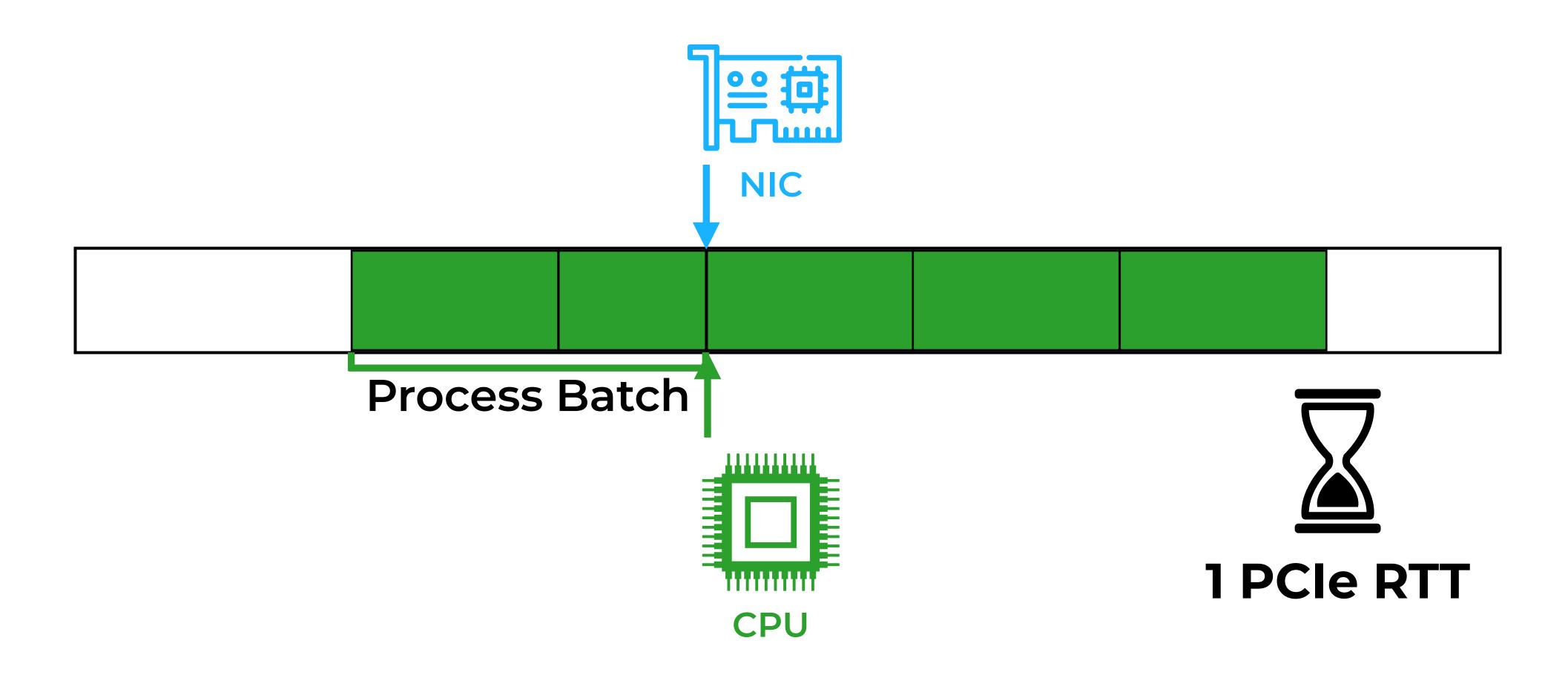


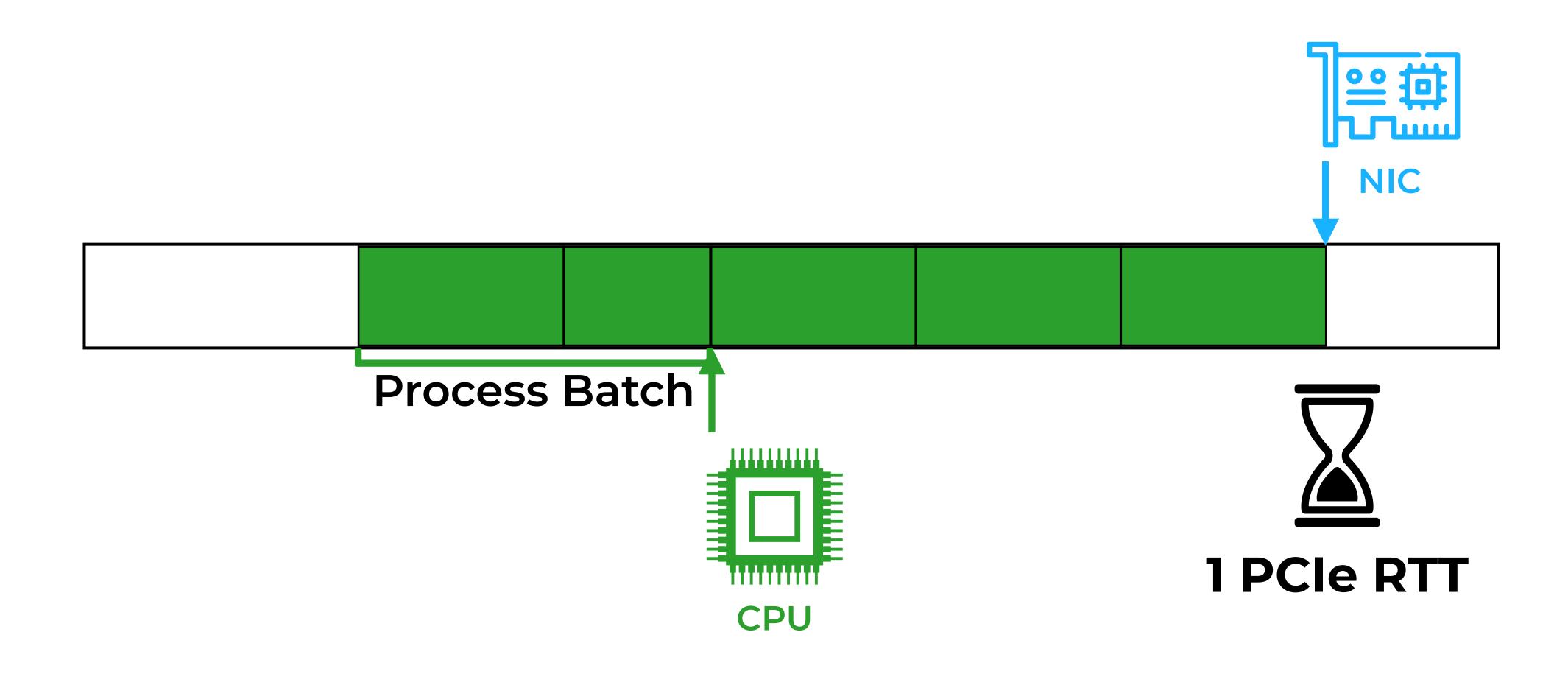
Only sends notifications that are strictly necessary

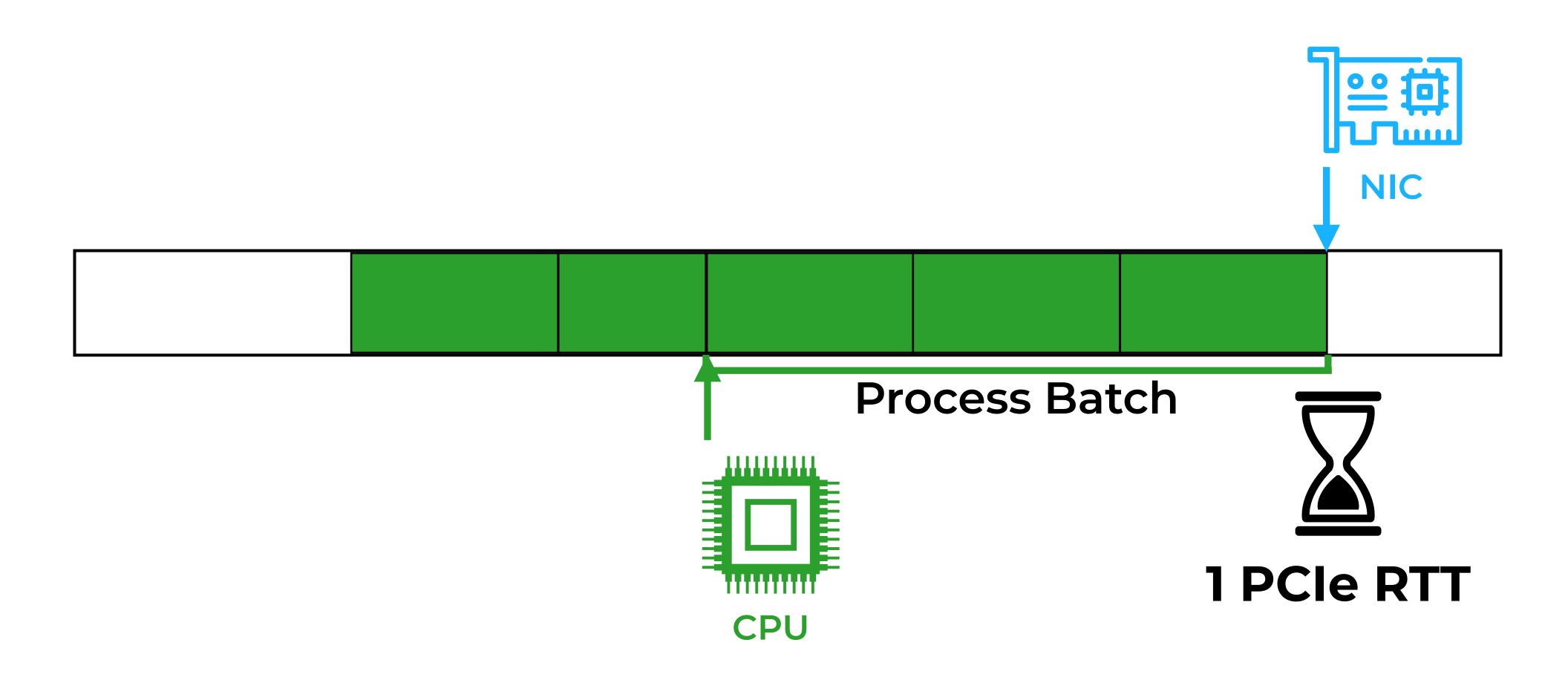


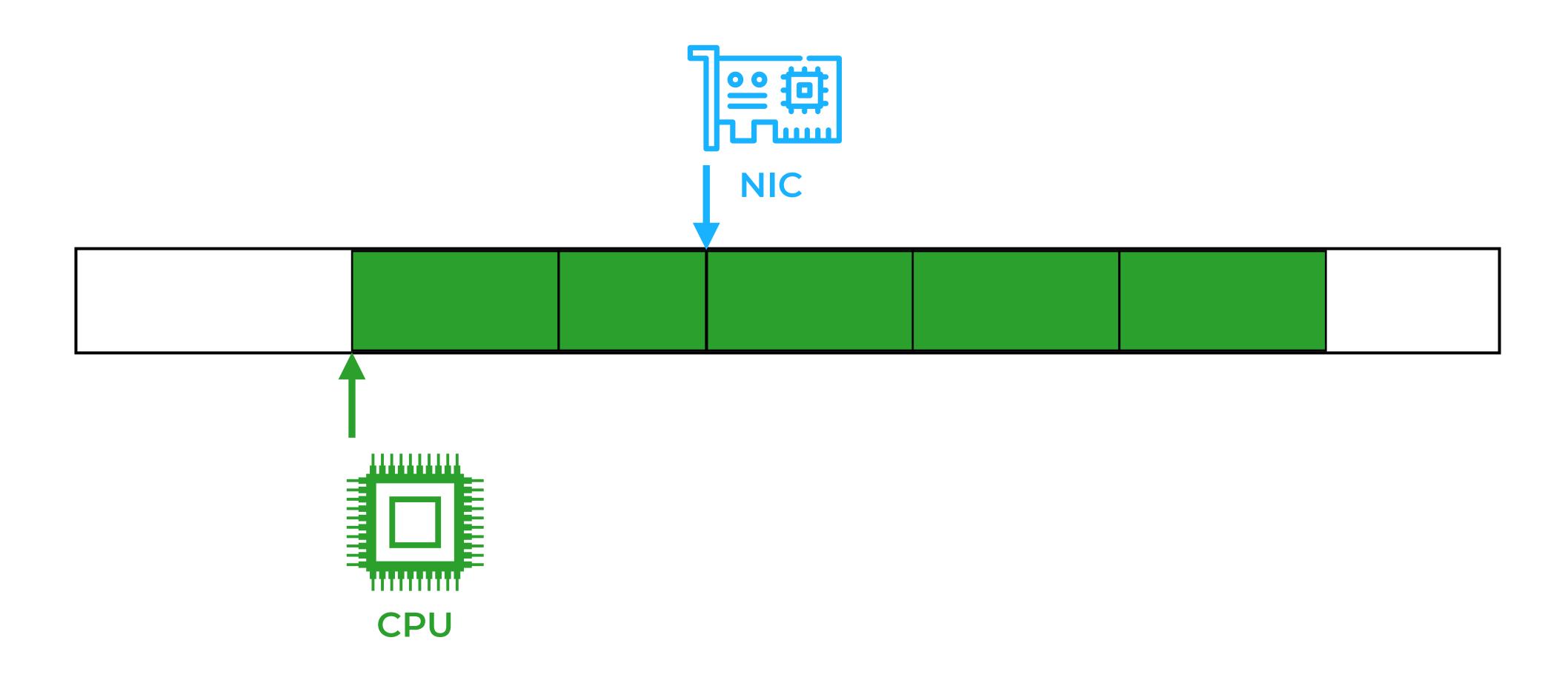


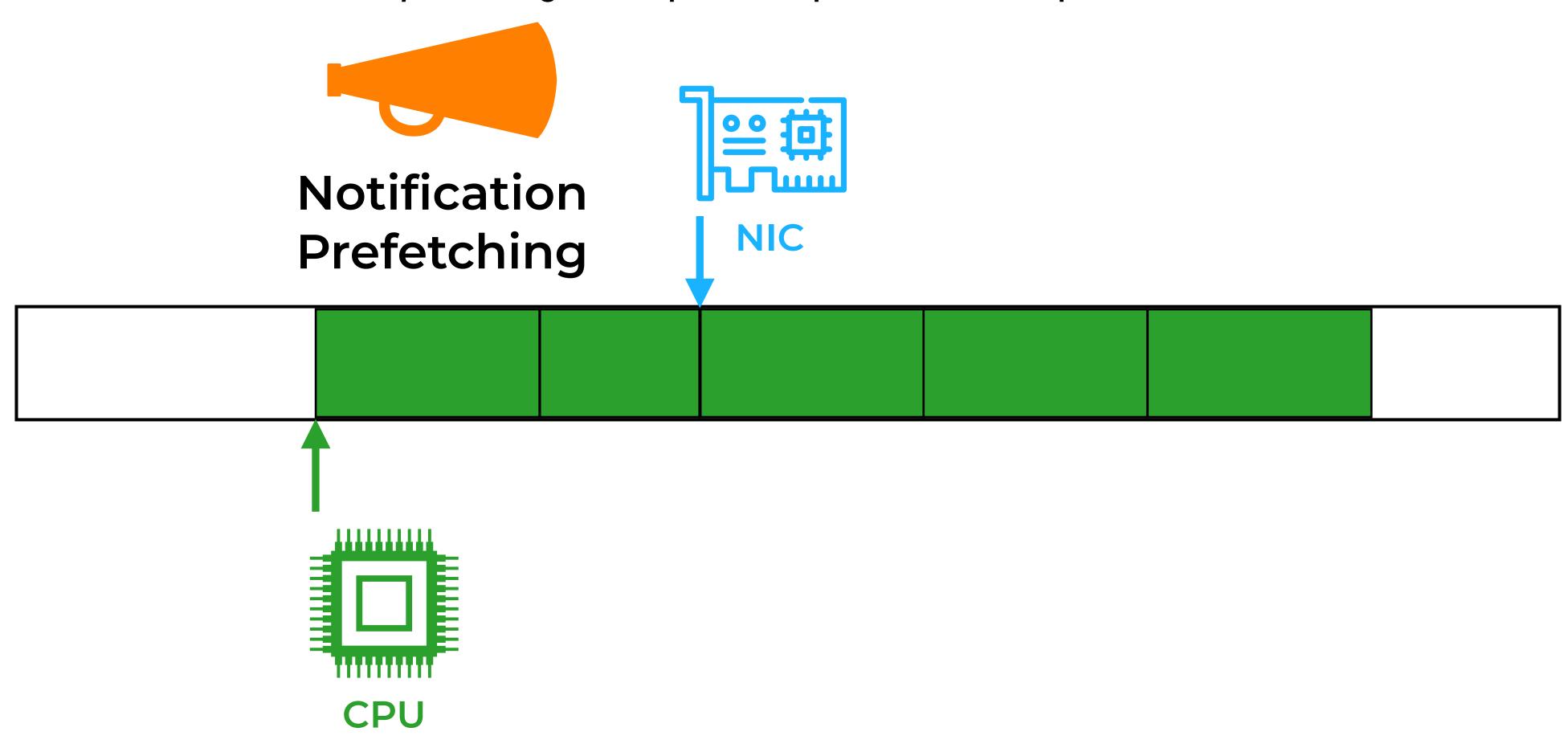


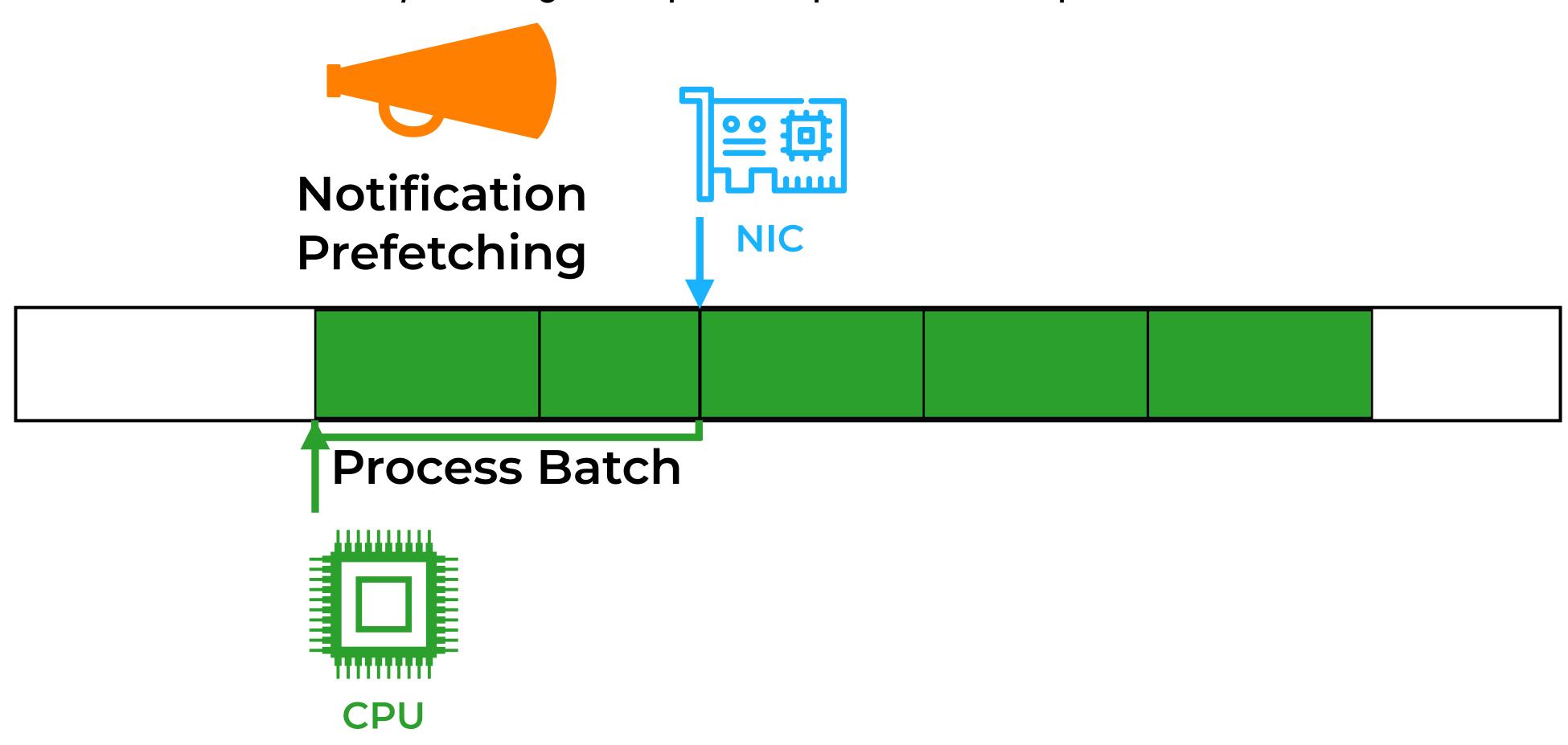


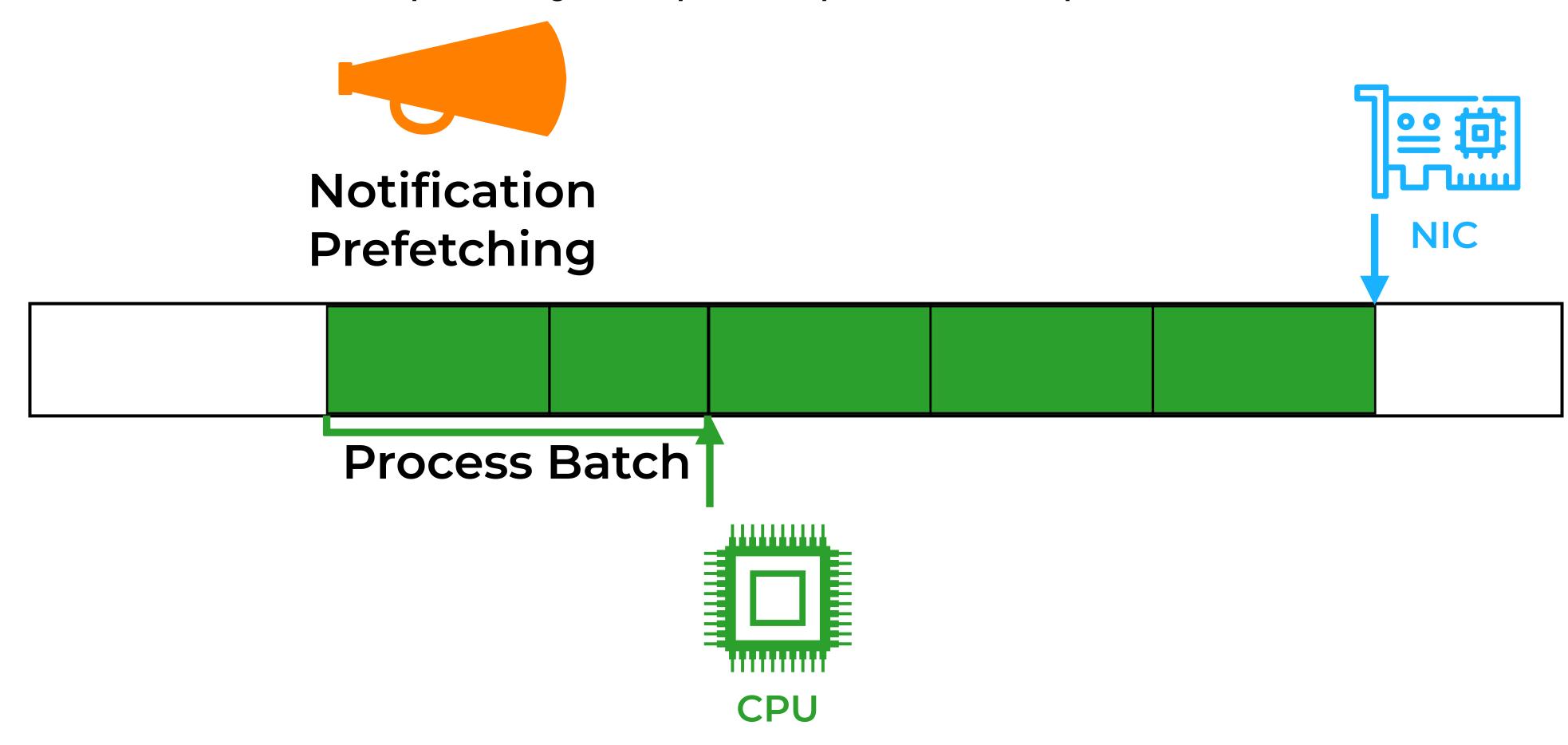


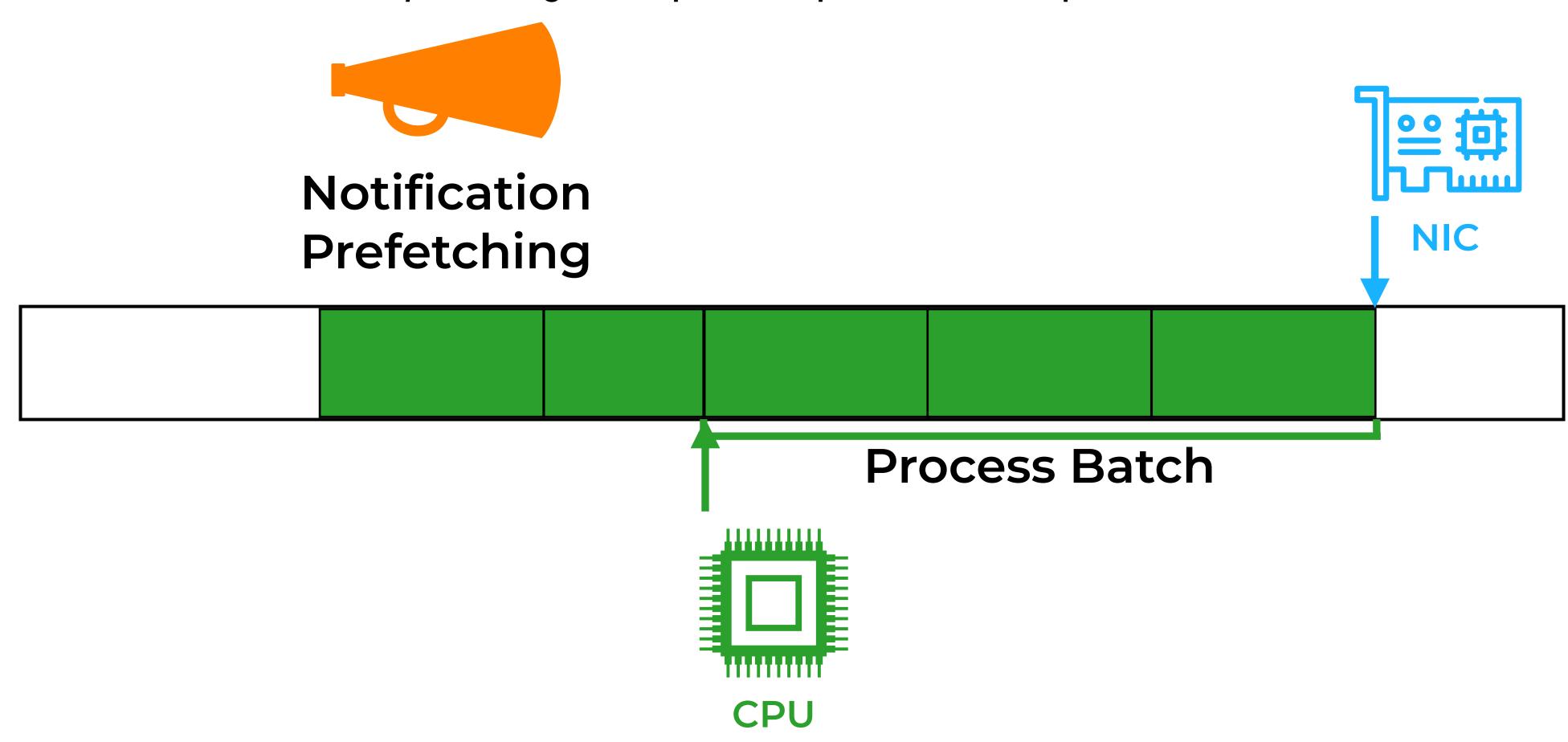












Many other design challenges...

How to notify pointer updates efficiently?

How to deal with data that wrap around?

How to design a scalable hardware?

How to avoid copies in applications that send data back (e.g., Network Functions)?

Many other design challenges...

How to notify pointer updates efficiently?

How to deal with data that wrap around?

How to design a scalable hardware?

How to avoid copies in applications that send data back (e.g., Network Functions)?

Refer to the paper for details

Ensō Implementation

Hardware Software CPU FPGA

Ensō Implementation

Hardware

Software

CPU

FPGA

Ensō NIC
(SystemVerilog)

Ensō Implementation

Hardware

Software

FPGA

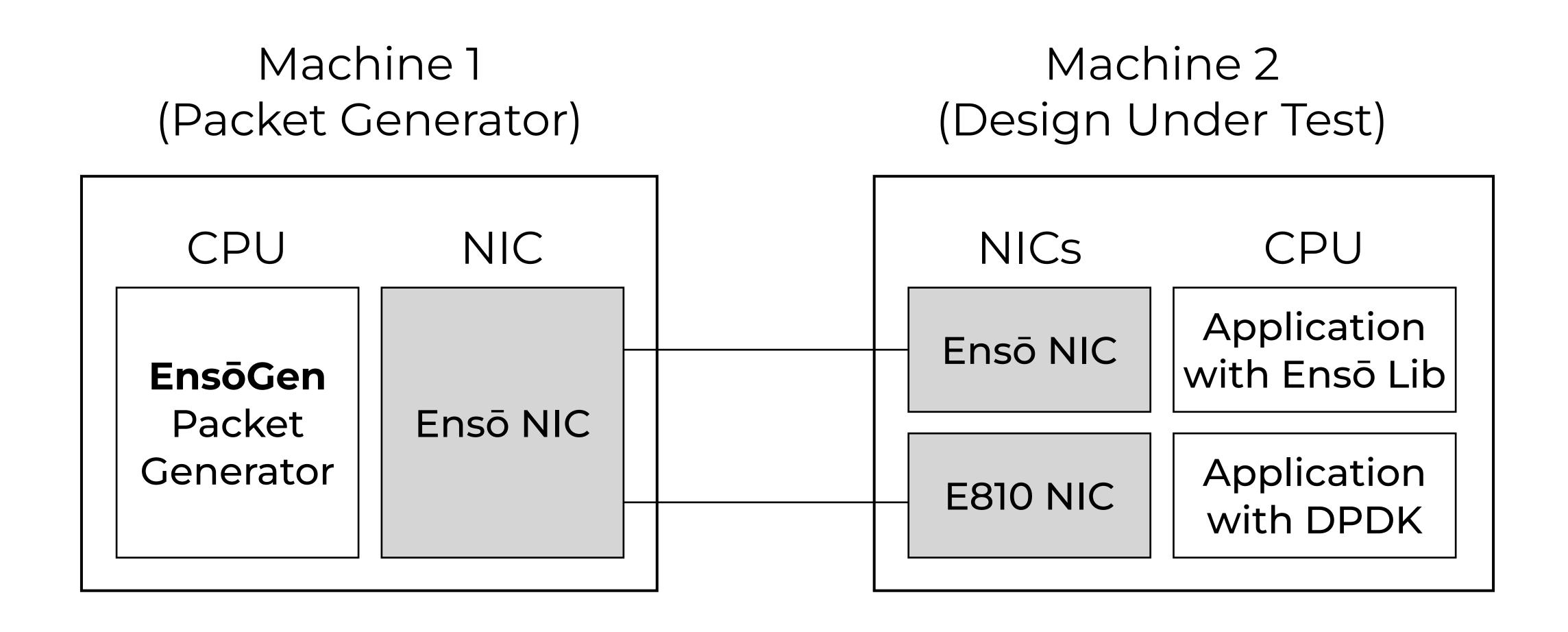
Ensō NIC
(SystemVerilog)

CPU

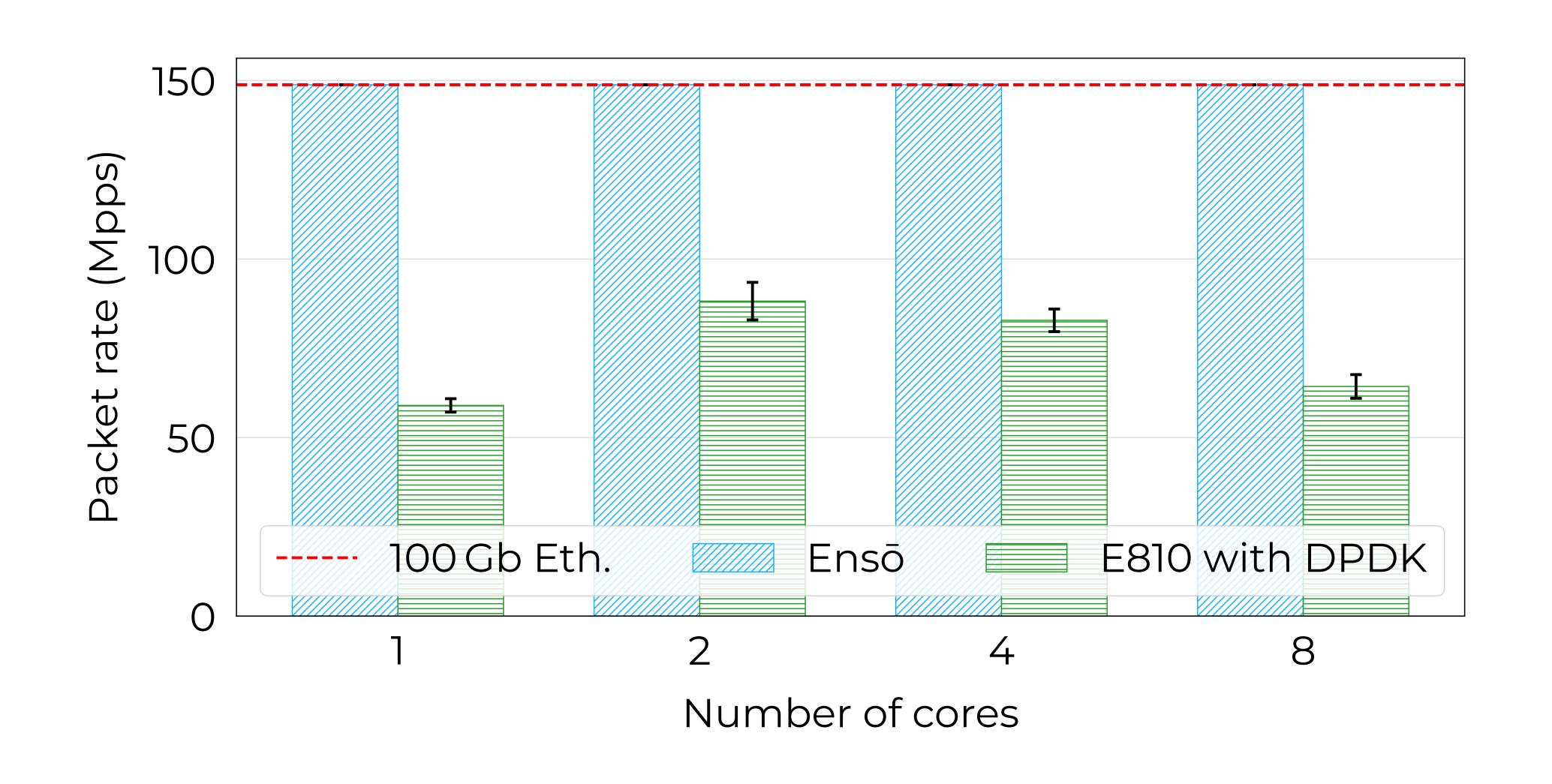
Kernel Module (C)

Ensō Library (C++17)

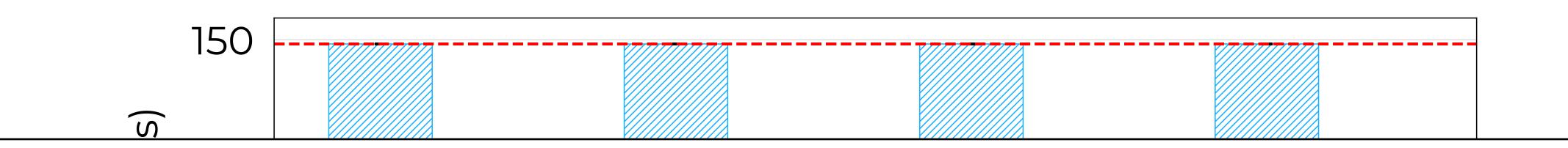
Evaluation



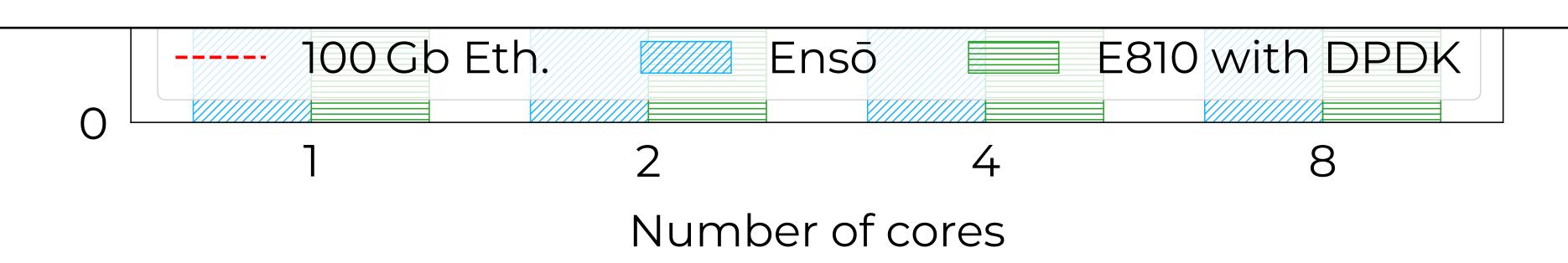
Ensō achieves 100 Gbps line rate (148.8 Mpps) using a single core



Ensō achieves 100 Gbps line rate (148.8 Mpps) using a single core



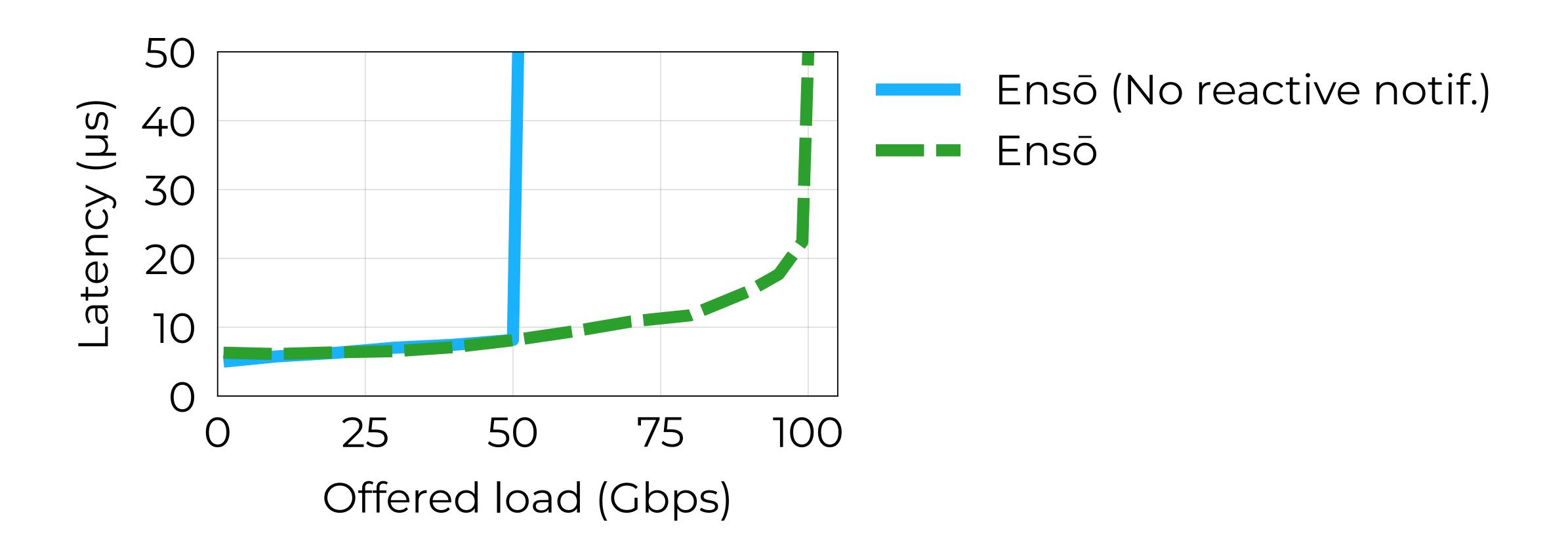
"Impressive results. Soundly destroys DPDK for many of the types of microbenchmark applications that are popular in the academic literature [...]" — Reviewer D



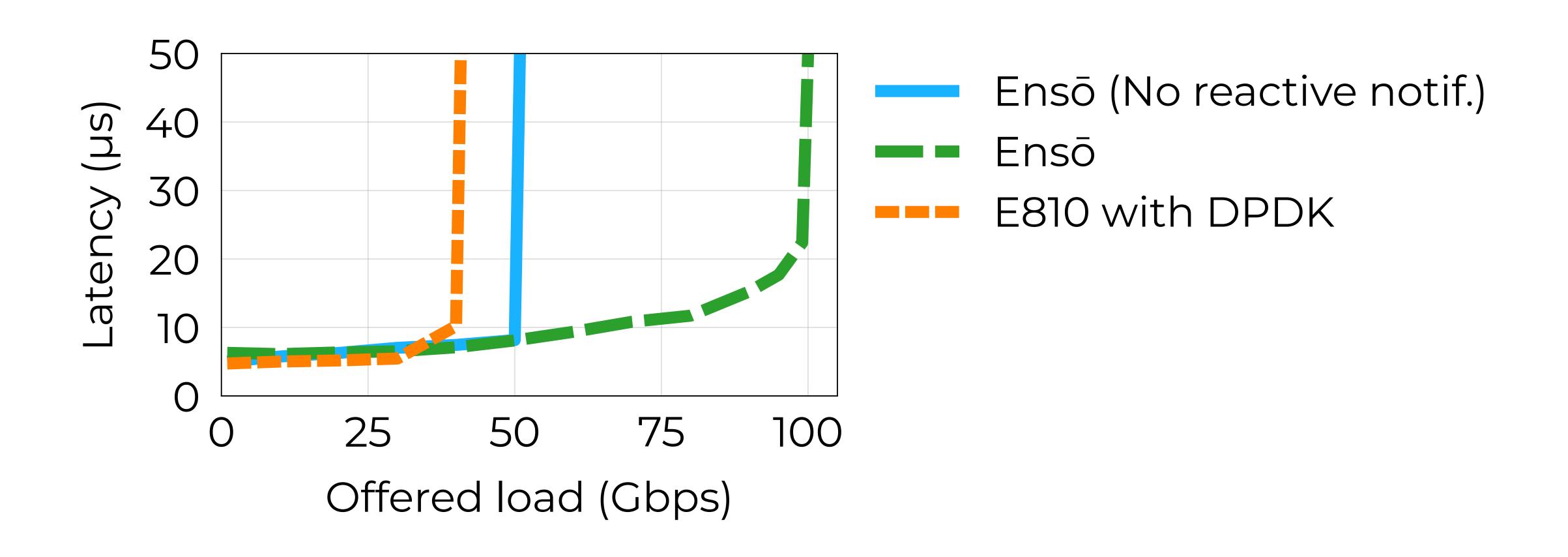
Ensō improves application throughput by up to 6x

Application	Throughput Improvement
Maglev Load Balancer [NSDI '16]	Up to 6x
Network Telemetry with NitroSketch [SIGCOMM '19]	Up to 3.5x
MICA Key-Value Store [NSDI '14]	Up to 47%
Log Monitor	Up to 95%

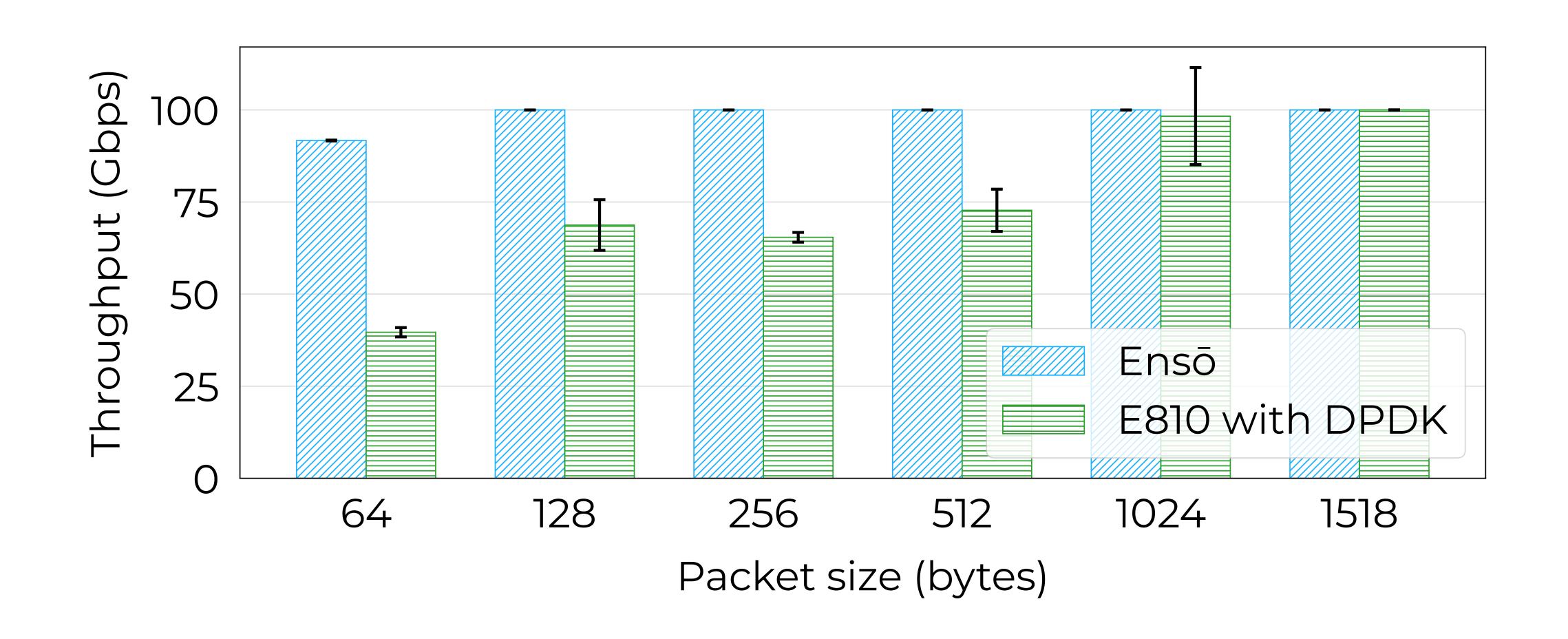
Reactive Notifications + Notification Prefetching improve throughput without impairing latency



Ensō achieves similar latency to the E810 NIC with DPDK, while sustaining a much greater load



Ensō outperforms the packetized interface even when copying data



Ensō is a streaming interface for NIC-Application communication

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Improves application throughput by up to 6x even with no offloads

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Allows easier and more efficient high-level offload implementations

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Ensō is open source: enso.cs.cmu.edu

Contact: sadok@cmu.edu